

Compal Confidential

FH5AT/FH4AT MB Schematic Document

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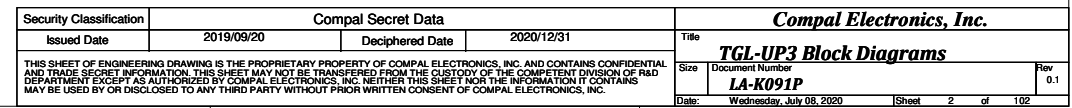
LA-K091P

Rev: 1.B

2020.07.08

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Project Name: LA-K091P



Board ID Table for AD channel

Vcc		3.3V			
Ra		100K +/- 1%			
Board ID /PCB Revision	Rb	V _{BI} D	min	V _{BI} D	TYP
0 --> 0.1	0			0 V	0.300 V
1 --> 0.2	12K +/- 1%		0.347 V	0.354 V	0.36 V
2 --> 0.3	15K +/- 1%		0.423 V	0.430 V	0.438 V
3 --> 0.4	20K +/- 1%		0.541 V	0.550 V	0.559 V
4 --> 0.5	27K +/- 1%		0.691 V	0.702 V	0.713 V
5 --> 0.6	33K +/- 1%		0.807 V	0.819 V	0.831 V
6 --> 0.7	43K +/- 1%		0.978 V	0.992 V	1.006 V
7 --> 0.8	56K +/- 1%		1.169 V	1.185 V	1.200 V
					0x00 - 0x13
					0x14 - 0x1E
					0x1F - 0x25
					0x26 - 0x30
					0x31 - 0x3A
					0x3B - 0x45
					0x46 - 0x54
					0x55 - 0x64

HSIO Port Table (CPU)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	PCle4 #1	No use	NA	PCle interface
1	PCle4 #2			
2	PCle4 #3			
3	PCle4 #4			

HSIO Port Table (PCH)

HSIO Port	Capable	Port Allocation	PCIE CLK	NOTE
0	USB3.1 #1 / PCle #1	USB3.1 Type C	NA	USB3.1 interface
1	USB3.1 #2 / PCle #2	NA	NA	NA
2	USB3.1 #3 / PCle #3	USB3.1 Type A	NA	USB3.1 interface
3	USB3.1 #4 / PCle #4	USB3.1 Type A (with charger)	NA	USB3.1 interface
4	PCle #5	SSD (NGFF Key M)	CLK1 & CLKREQ#1	PCle interface
5	PCle #6			
6	PCle #7 /GbE			
7	PCle #8 /GbE			
8	PCle #9 /GbE	GLAN	CLK2 & CLKREQ#2	PCle interface
9	PCle #10	WLAN	CLK3 & CLKREQ#3	PCle interface
10	PCle #11 /SATA0	HDD	NA	SATA interface
11	PCle #12 /SATA1	ODD	NA	SATA interface

Load BOM Option Table

43#	FH4AT/ FH5AT	Load BOM Option
431AMXBOL01/ 431AMXBOL51		GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i3@/FP3V@/USBT5@/PCB@
431AMXBOL04/ 431AMXBOL52		GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i5@/FP3V@/USBT5@/PCB@
431AMXBOL03/ 431AMXBOL53		GSEN@/FP@/255@/CHG@/TPM@/PREM@/DVT@/MEM@/CNVi@/CMC@/GLITCH@/UMA@/3S@/ES2_i7@/FP3V@/USBT5@/PCB@

X4E/X76 X63/X4P	Load BOM Option
X76826BOL51	X76HYN4@/SDP@
X76826BOL52	X76MIC4@/SDP@
X76826BOL53	X76SAM4@/SDP@
X76826BOL54	X76HYN8@/DDP@
X4EAMXBOL01	FPEMC@/EMC@/

BOM Structure Table

HW Function	BOM Structure
UMA SKU	UMA@
CMC	CMC@
EMI / EMC / ESD	EMC@ XEMC@
RF Components	@RF@
Premium/Volume	PREM@ VOL@
CNVi	CNVi@
UART	UART@
CPU	ES2_i3@ ES2_i5@ ES2_i7@
Finger Print	FP@ FPEMC@ FP3V@ FP5V@
ODD	ODD@
GLITCH	GLITCH@
Touch screen I2C/USB	I2CTS@ USBTS@
Board ID	EVT@ DVT@ PVT@
TPM	TPM@
Gsensor	GSEN@
Charger	CHG@
over 3 cell battery	3S@
NC Components	@
MD BOM select	SDP@ X76SAM4@ X76HYN4@ X76MIC4@ DDP@ X76HYN8@ NODX76@
MD BOM select	MEM@
ME Connector	CONN@
Audio	255@ 256@ 255M@
PCB	PCB@

Power Function

Adaptor	45W@ 65W@
TEMP. protect	OTP@
4 cell battery	4S_BATT@
EMI	EMI@ @EMI@
RF Components	@RF@

SOC SMBUS Address Table (TBC)

SOC_SMBUS Net Name	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
SOC_SMBCLK SOC_SMBDATA	+3V_PRIM level shift to +3VS	DIMM1	TBC	TBC	0xA0
		G-sensor	TBC	TBC	0xA4
SOC_SML0CLK SOC_SML0DATA	+3V_PRIM	NC	TBC	TBC	TBC
SOC_SML1CLK SOC_SML1DATA	+3V_PRIM	EC	TBC	TBC	TBC
		NC	TBC	TBC	TBC

EC SMBUS Address Table

EC_SMBUS Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
EC_SMB_CK1 EC_SMB_DA1	+3VLP_EC	BAT	0x16	TBC	TBC
		CHGR	0x12	TBC	TBC
EC_SML1CLK EC_SML1DATA	NC	NC	TBC	TBC	TBC

I2C Address Table (TBC)

I2C Port	Power Rail	Device	Address (7 bit)	Address (8bit)	
				Write	Read
I2C 0	NC	NA	0x0FH	TBC	TBC
I2C 1	NC	NA	0x48H	TBC	TBC
I2C 2	NC	NA	TBC	TBC	TBC
I2C 3	+3VS	Touch Pad	0x2CH	TBC	TBC
I2C 4	NC	NA	0FH	TBC	TBC
I2C 5 ISH_I2C 2	+3VS (need check)	Touch Screen (I2C interface)	TBC	TBC	TBC
ISH_I2C 0	NC	NA	TBC	TBC	TBC
ISH_I2C 1	NC	NA	TBC	TBC	TBC

Voltage Rails


Power Plane	Description	S0	S0ix	S3	S4/S5
+19V_ADPIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT+	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit	N/A	N/A	N/A	N/A
+VCCIN	Core voltage for CPU	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+1.05V_VCCST	Sustain voltage for CPU standby modes	ON	ON	ON	OFF
+1.05VS_VCCSTG	Gated sustain voltage for CPU standby modes	ON	OFF	OFF	OFF
+1.2V_VDDQ	DDR4/L-RS +1.2V power rail and CPU digital PLL	ON	ON	ON	OFF
+2.5V	DDR4/L-RS +2.5V power rail	ON	ON	ON	OFF
+1.8VALW_PRIM	TCSS/AGSH TypeC sub system / CPU analog power supply	ON	OFF	OFF	OFF
+1.8VALW	System +1.8V power rail	ON	ON	ON	ON*
+1.8VS	System +1.8VS power rail	ON	ON	OFF	OFF
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+3VALW	+3VALW power for PCH DSW rails	ON	ON	ON	ON*
+3V_PRIM	+3VALW power for PCH suspend rails	ON	ON	ON	ON*
+3VS	System +3VS power rail	ON	ON	OFF	OFF
+1.8VS_DGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VS_DGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+VGA_CORE	Power rail for GPU	ON	OFF	OFF	OFF
+5VALW	System +5VALW power rail	ON	ON	ON	ON*
+5VS	System +5VS power rail	ON	ON	OFF	OFF
+3VL_RTC	RTC power	ON	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

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FQA01 Schematic: LA-H891PR01_0401A



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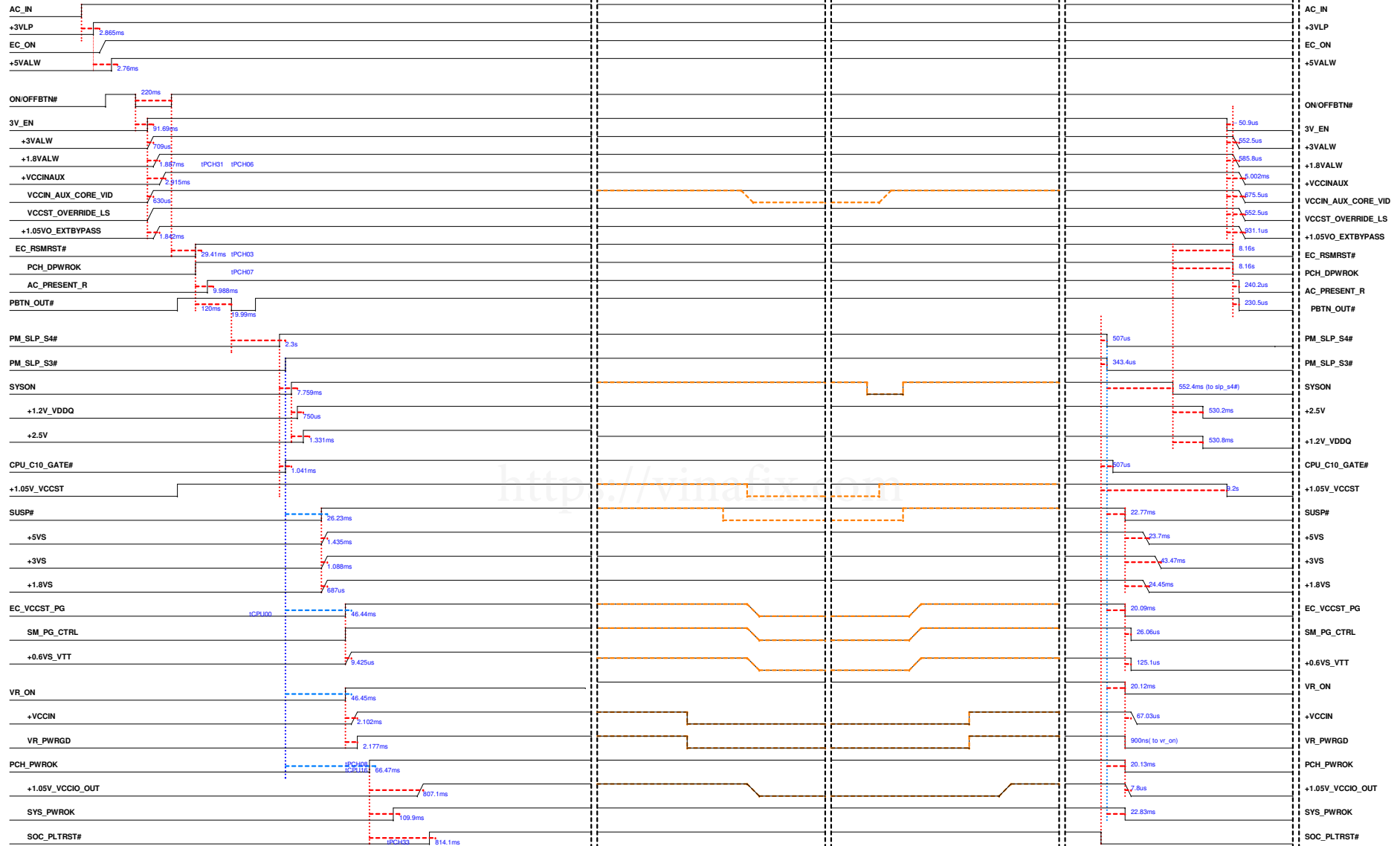
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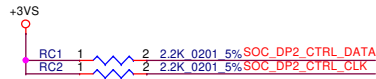
G3->S0

S0-> S0iX

S0iX ->S0

S0->S5





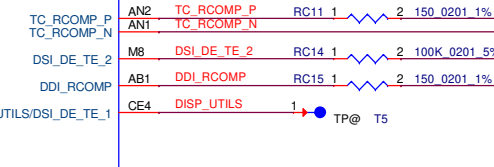
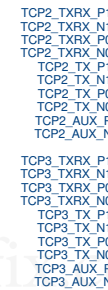
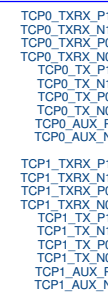
PCB DAZ

ZZZ

LA-K091/LS-K091/LS-K096
PCB FH5AT LA-K091P LS-K091P/K096P
DAZ34G00203
PCB@



TGL-U_BGA1449



Tiger Lake-UP3 CPU SKU

i7-1165G7-QVBA



TGL-UP3_BGA1449
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SA0000DRG30
QS_I7@

i5-1135G7-QVBD

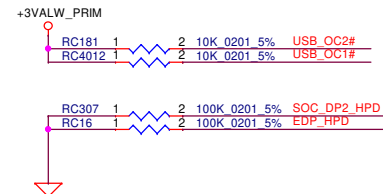


TGL-UP3_BGA1449
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QS_I5@

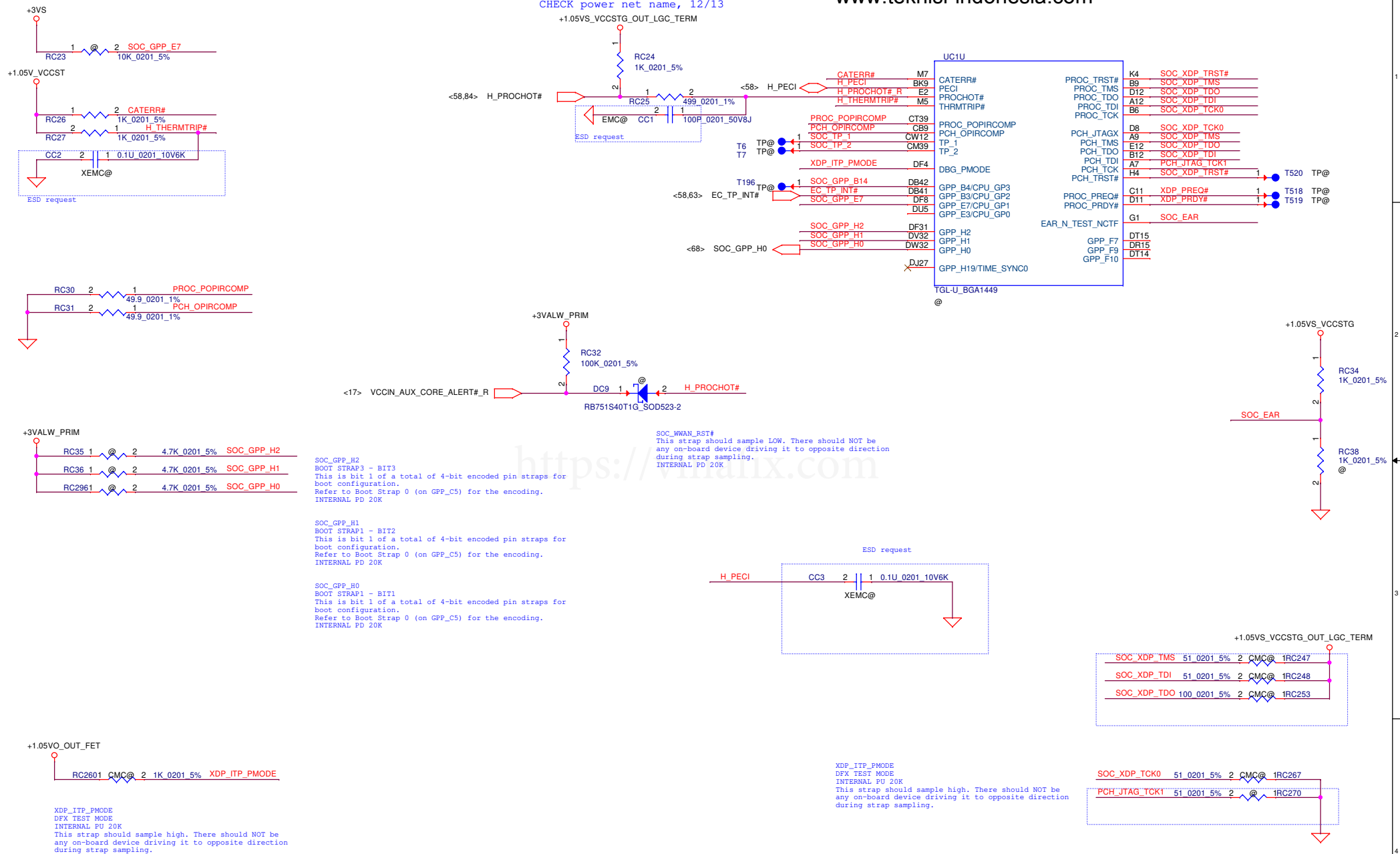
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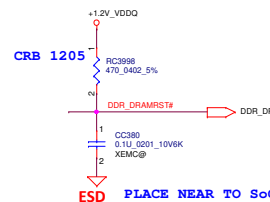
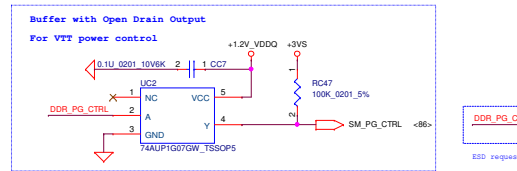
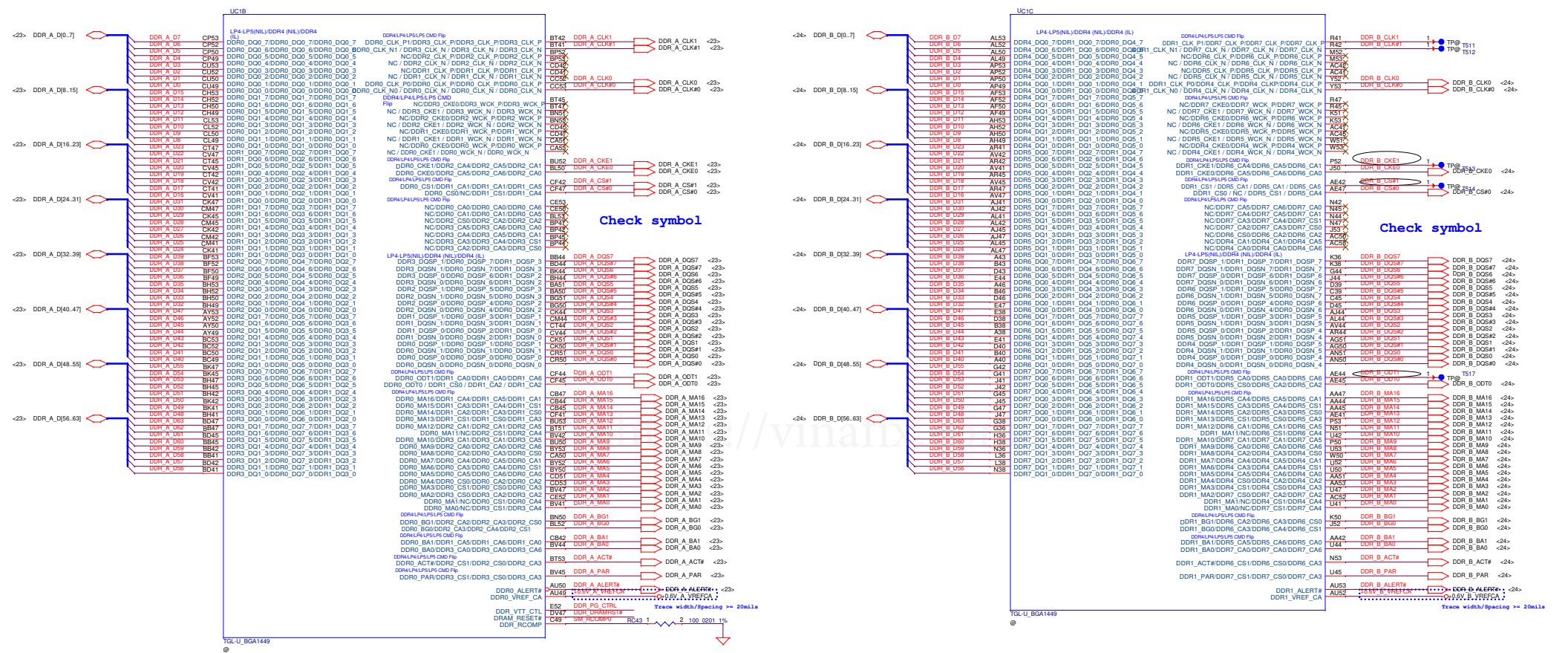
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								Date:		Wednesday, July 22, 2020	



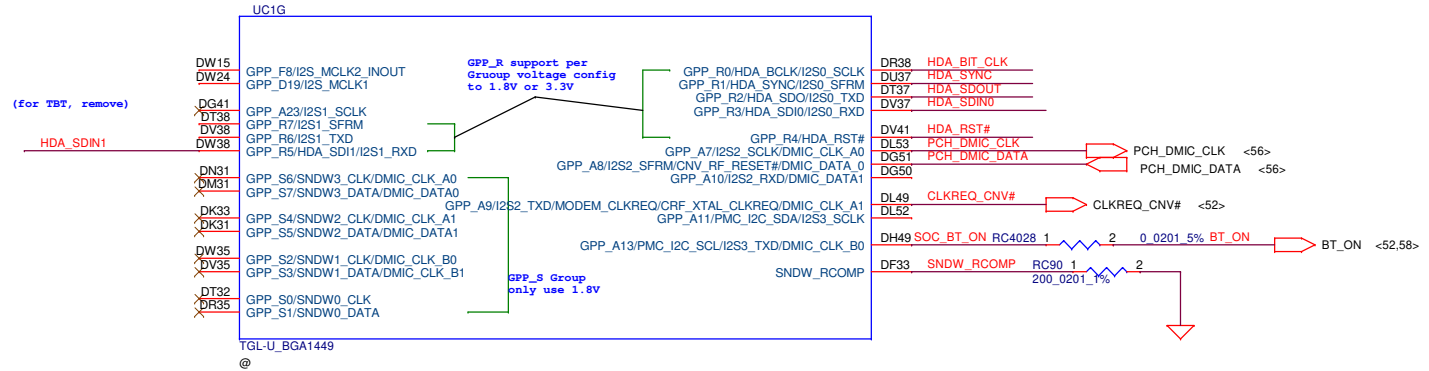
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Follow Intel DDR4 NIM

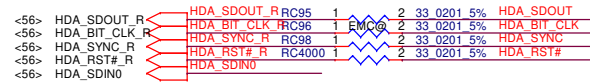
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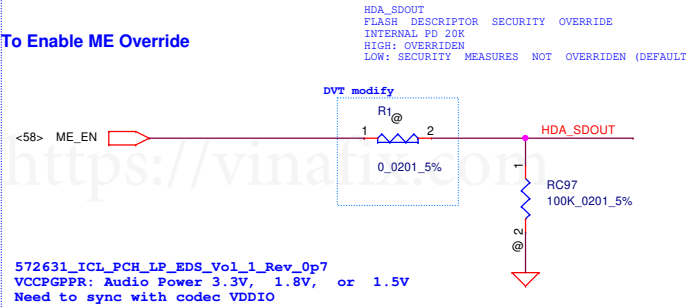
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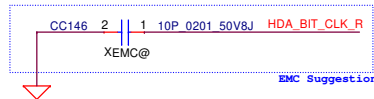
HDA for AUDIO



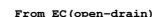
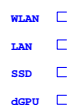
To Enable ME Override




Follow
607872_TGL_UY_PDG for Glitch



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PDG 6.8.6
For Integrated Bluetooth* functionality with the Intel® Wireless-AC (CNVi) solution,
Tiger Lake PCH-LP USB 2.0 port # 10 must be used.

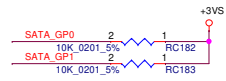
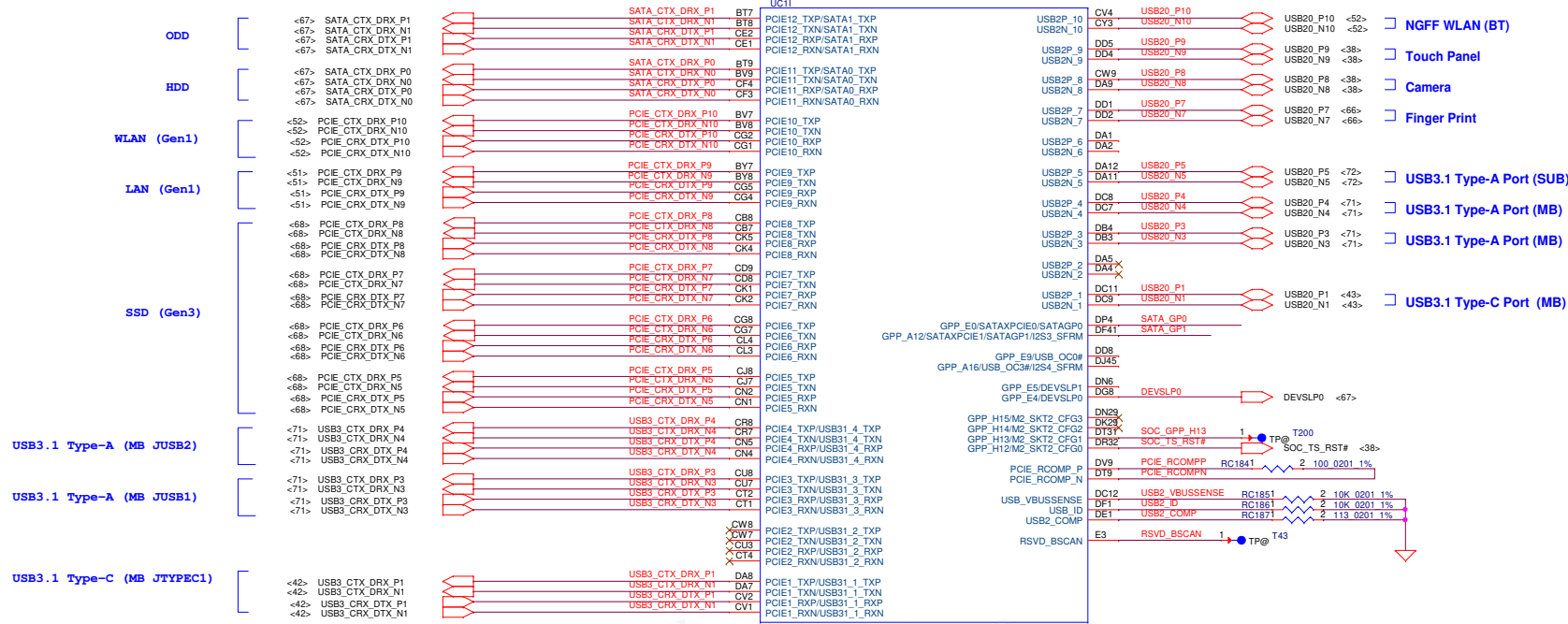


Figure 70. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

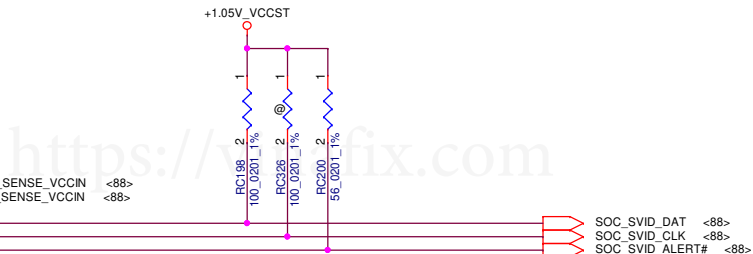
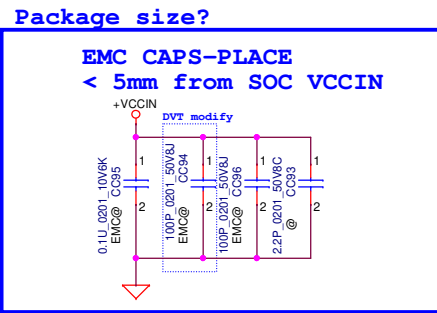
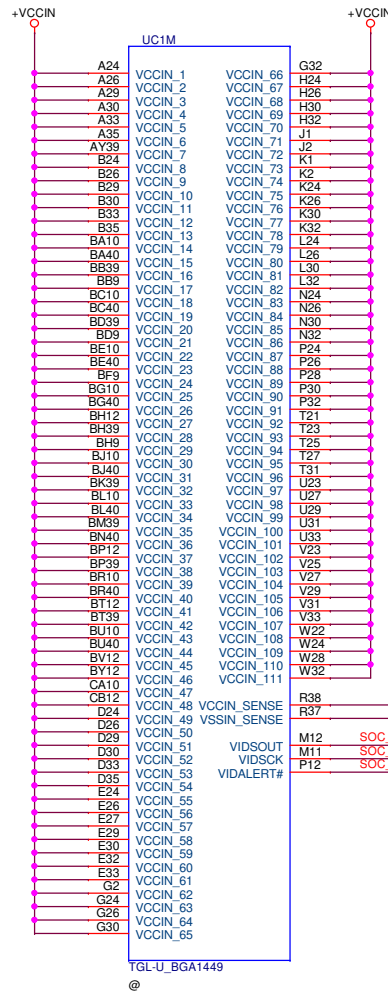
Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/Zx1 #1	USB 3.2 Gen 1x1/Zx1 #2	USB 3.2 Gen 1x1/Zx1 #3	USB 3.2 Gen 1x1/Zx1 #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12
	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4			GPE	GPE	GPE			SATA 1

DIS dGPU function, remove

DIS dGPU function, remove

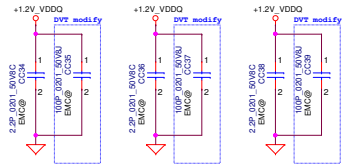
Table 58. Signal Descriptions

Name	Type	SSC Capable	Description
PCH-LP (U):			
• CLKOUT_PCIE_P[6:0]			
• CLKOUT_PCIE_N[6:0]			
PCH-LP (Y):			
• CLKOUT_PCIE_P[6:1]			
• CLKOUT_PCIE_N[6:1]			

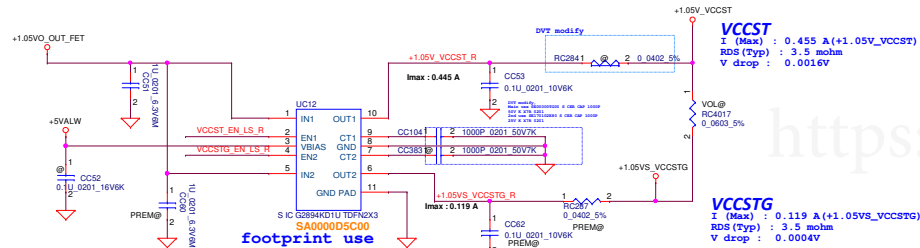
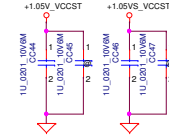
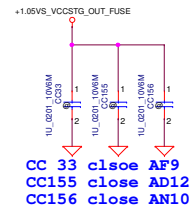
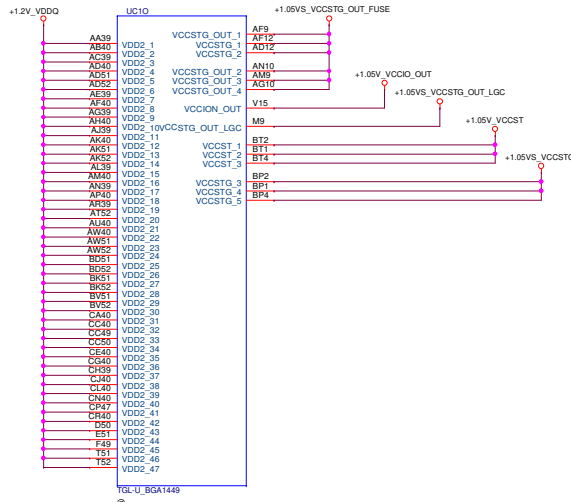
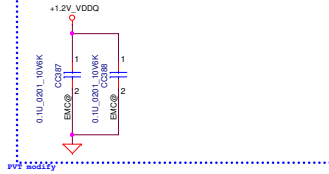


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EMC CAPS-PLACE
< 4mm from SOC VDDQ
with each pair < 12mm Apart
12pF* 3 (EMC@)
2.2pF* 3 (EMC@)



ESD request only for LA-K091
Add 2*0.1u CAP for +1.2V_VDDQ
near PJM3
TOP*1 BOT*1



VCCST
I (Max) : 0.455 A(+1.05V_VCCST)
RDS (Typ) : 3.5 mohm
V drop : 0.0016V

VCCSTG
I (Max) : 0.119 A(+1.05V_VCCSTG)
RDS (Typ) : 3.5 mohm
V drop : 0.0004V

Place on CPU Side
1uF* 10
10uF* 16
47uF * 2

CPU_C10_GATE# stable to +1.05VS_VCCSTG <= 65us (ICPU26)

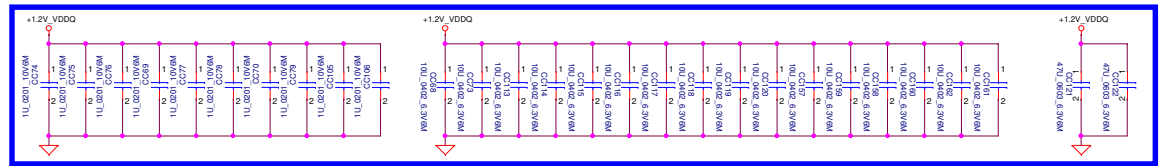


Figure 228. VCCST Enable Logic

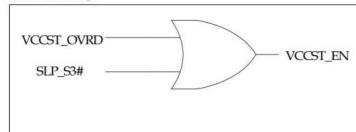
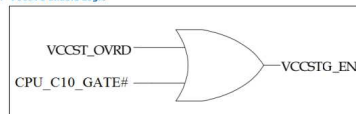
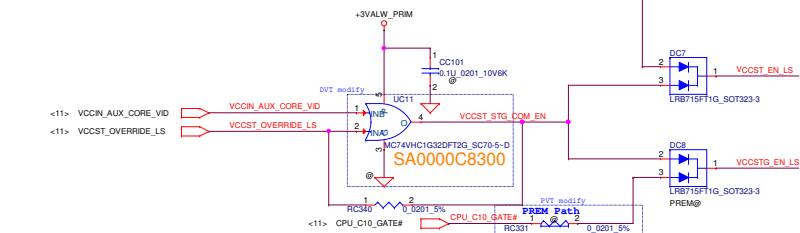


Figure 229. VCCSTG Enable Logic

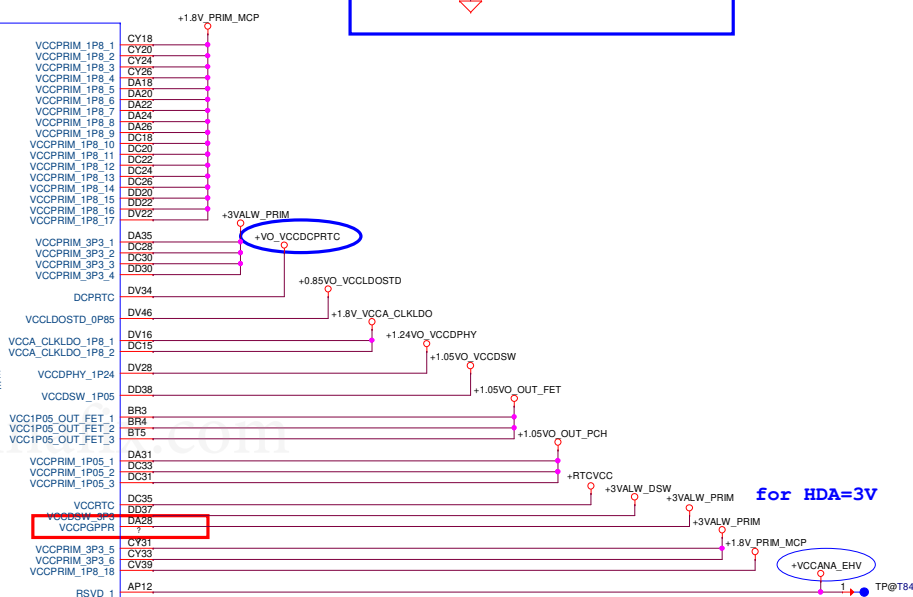
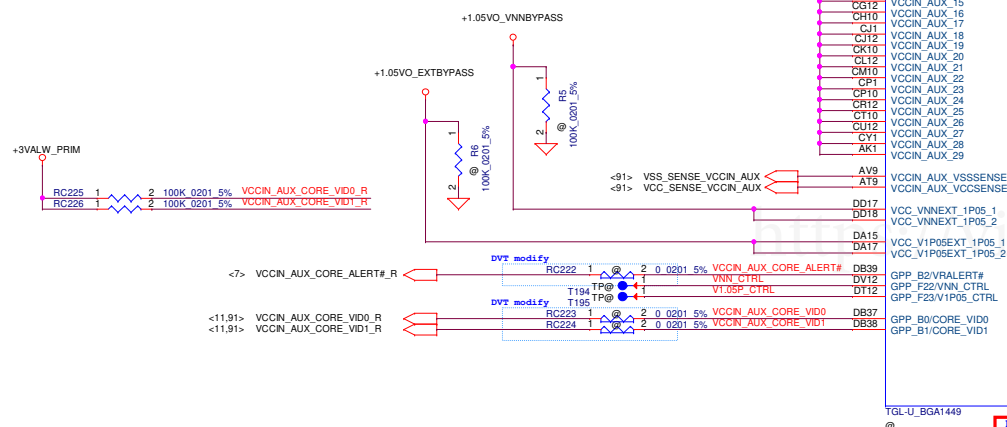
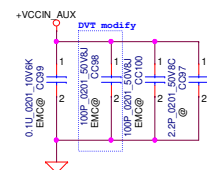
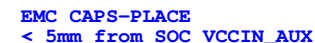
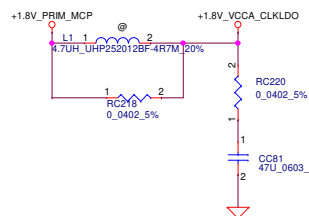


VCCST/VCCSTG Enable

ICL have EC_VCCST_EN
check need it? or use syson/susp? 1210

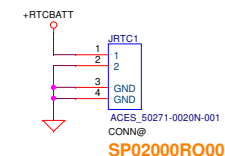
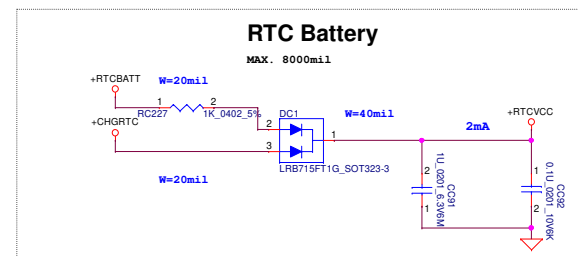
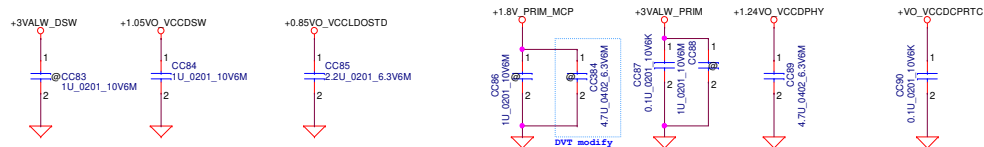


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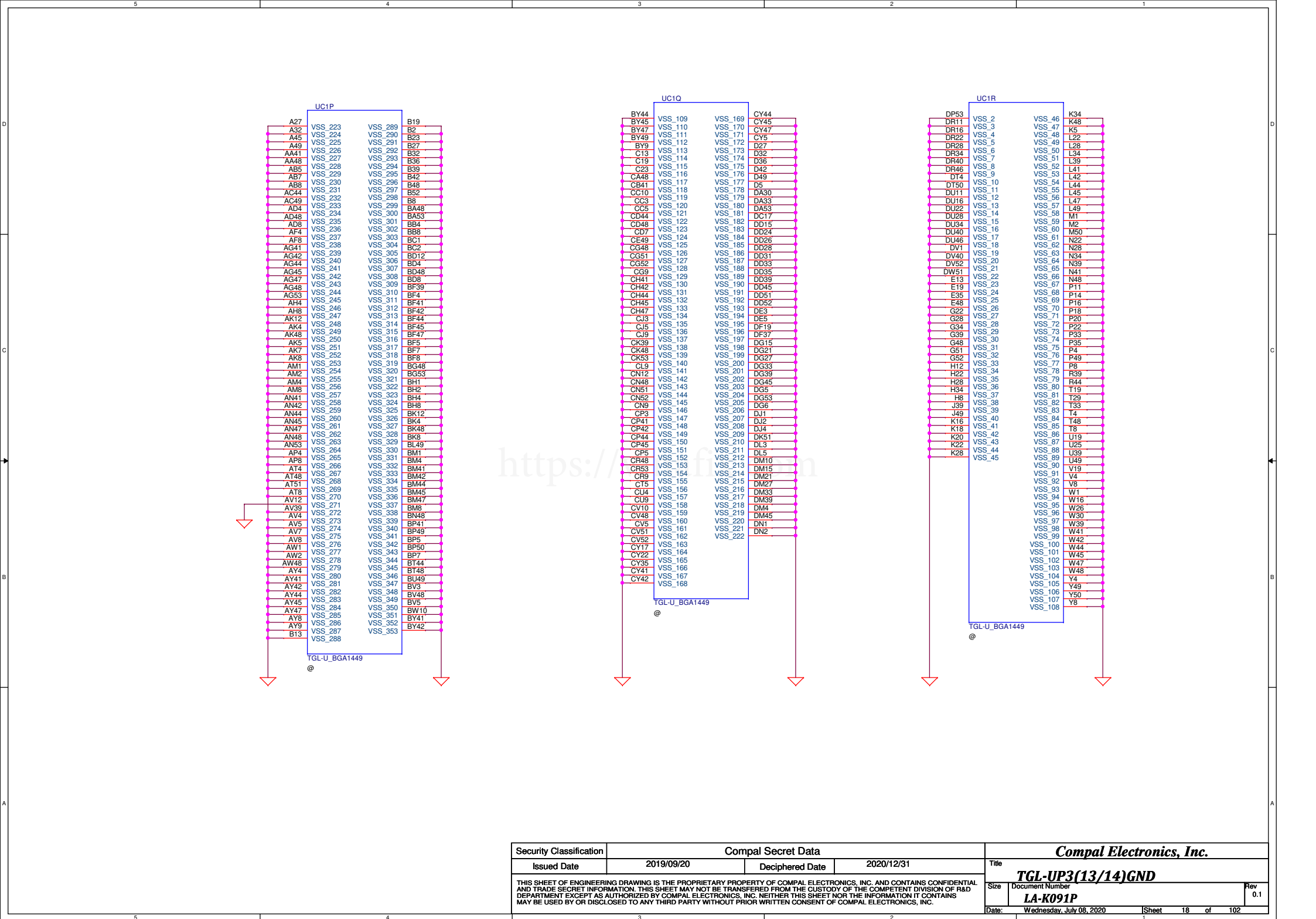


NOTE:
576591-tgl-pch-lp-eds-vollof2-rev0p5
VCCPGPPR: Audio Power 3.3V, 1.8V, or 1.5V
Need to sync with codec VDDIO.

607872_TGL_UY_PDG_Rev0p5
When configured as 3.3V or 1.8V, VCCPGPPR can be merged directly with
either VCCPRIM1P8 or VCCPRIM3P3 depending on their operating voltage.



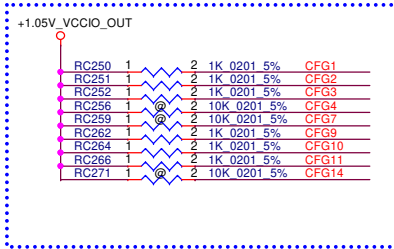
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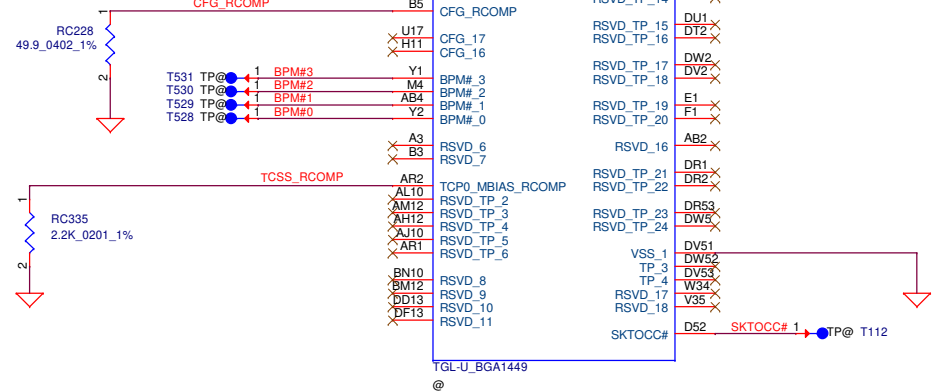
CFG	Description	Termination	Resistor
	Operation: No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 - (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[17:15]	RSVD	None	

CFG4
Display port presence strap
LOW : Enable
An external display port device is connected to the embedded displayport
HIGH : Disable
No physical display port attached to embedded display port

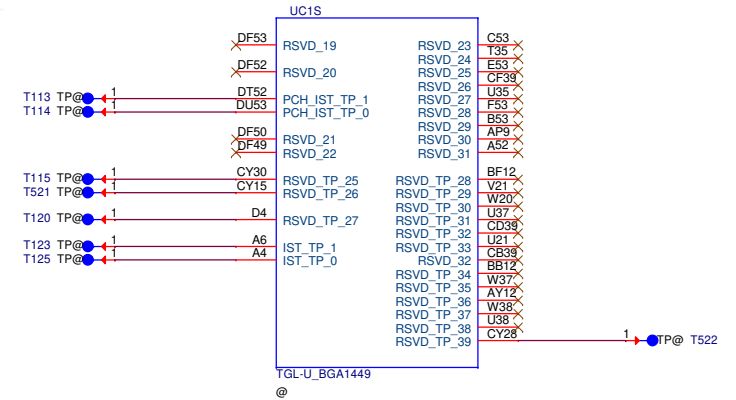
CFG7
PEG Training
LOW : PEG Wait for BIOS for training.
HIGH : (default) PEG Train immediately following RESET# de assertion.



CFG Signals (For Strap & XDP)



0109 remove ES1@ componet



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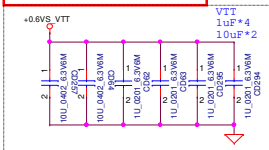
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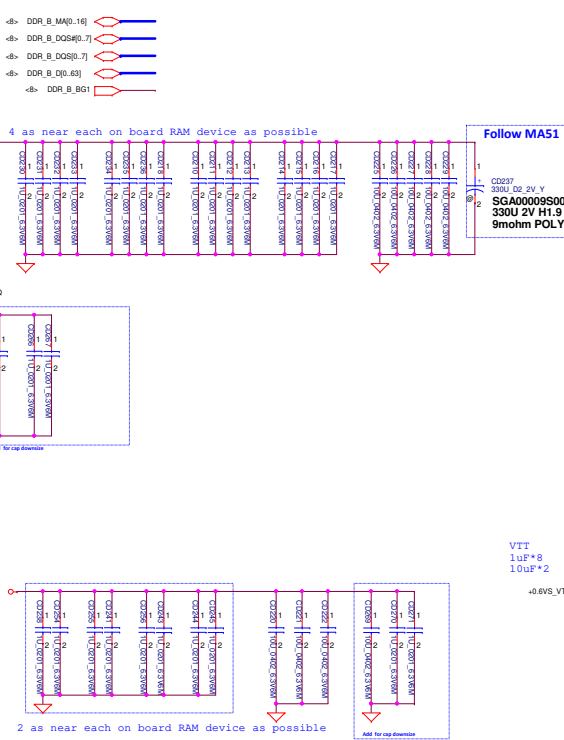
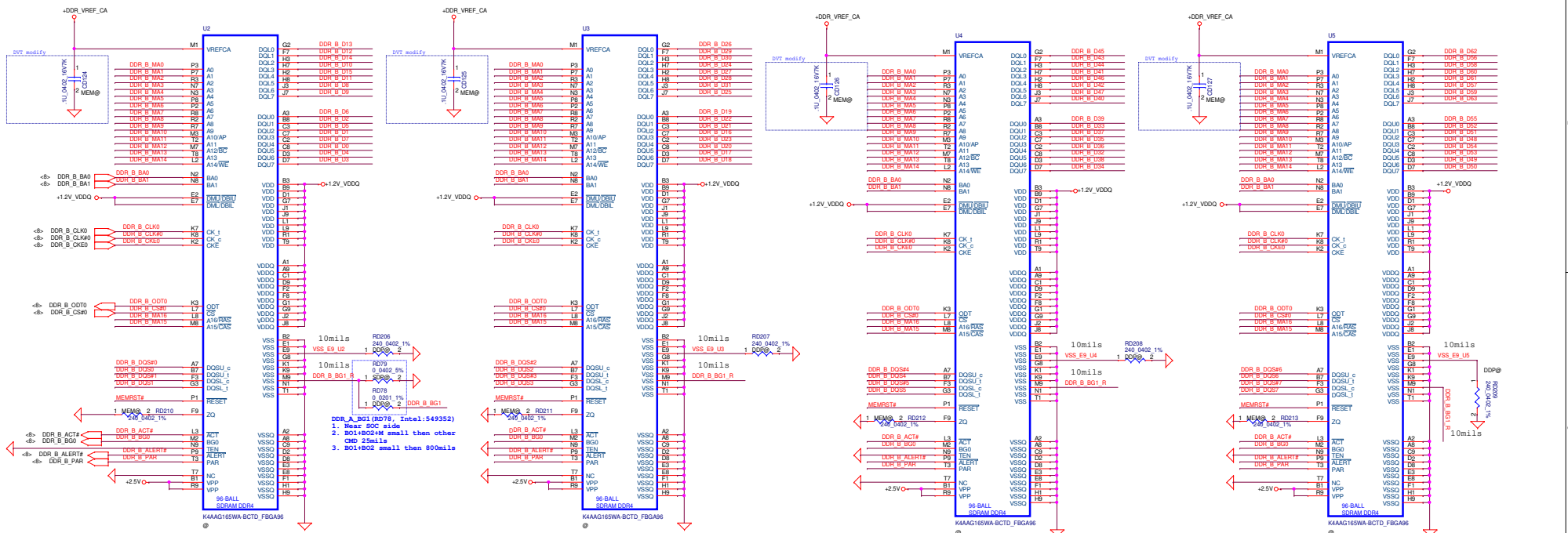
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Note: 1. Total quantity is referring to 2 channels

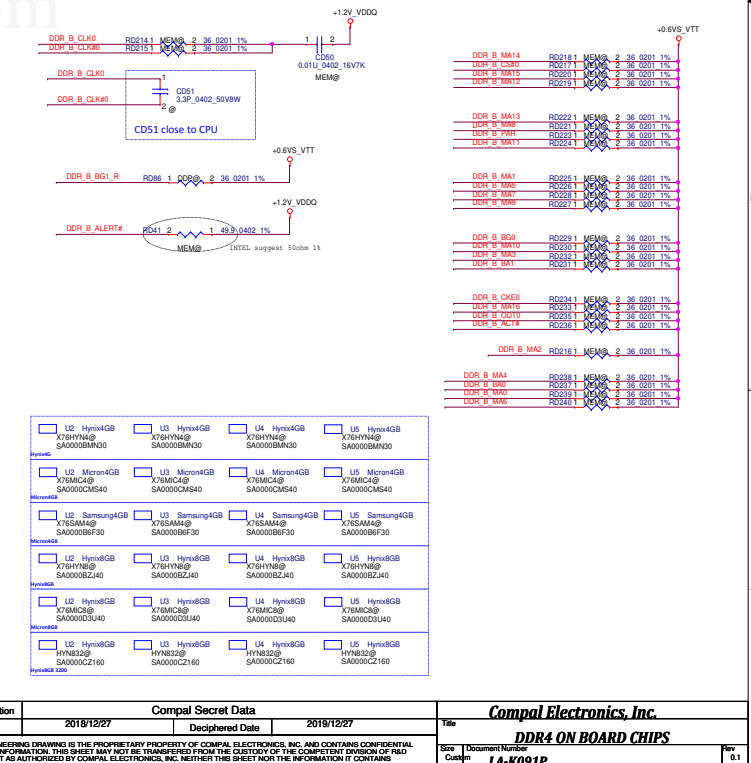
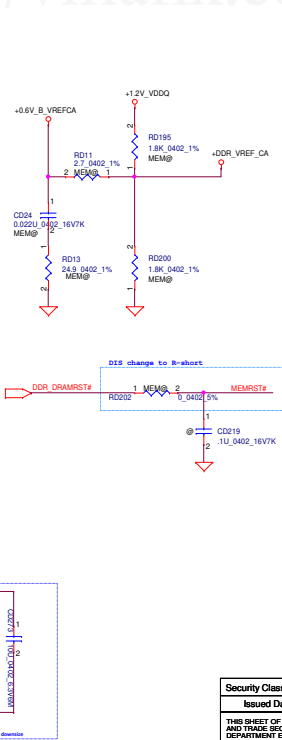
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DDR4 mapping	SDP	DDP
E9	VSS	U2Q
M9	VSS	BG1
T7	VSS	VSS

RCOMP(0) (SOC side) 200_1% 121_1%

SDP# RD200 0.0402 5% SD028000080
SDP# RD201 0.0402 5% SD028000080
SDP# RD202 0.0402 5% SD028000080
SDP# RD203 0.0402 5% SD028000080



TERMINATION

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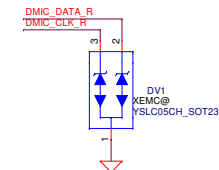
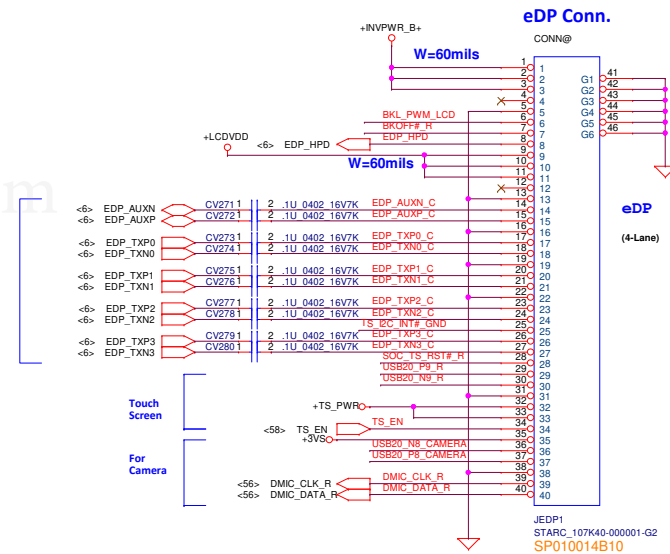
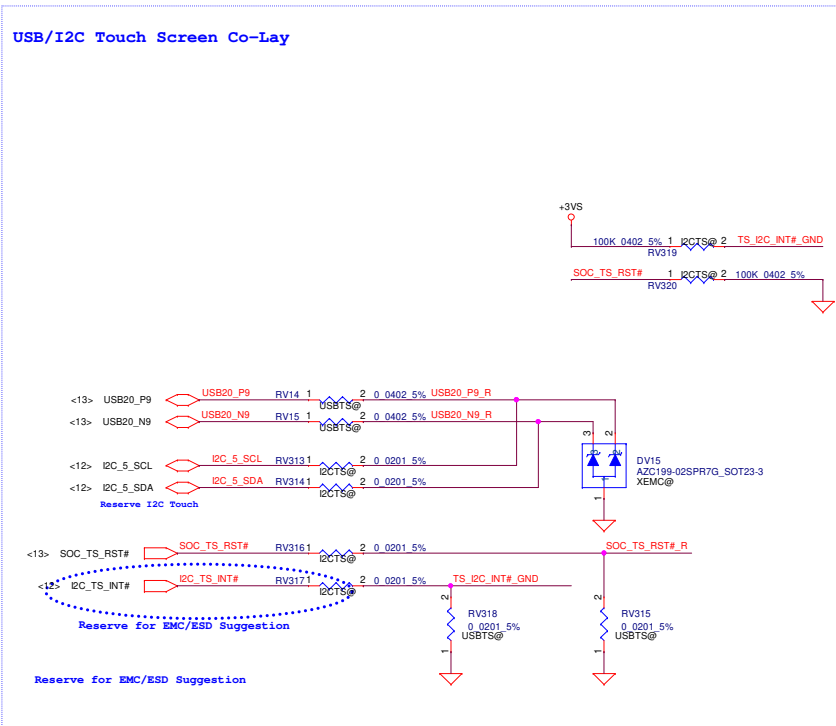
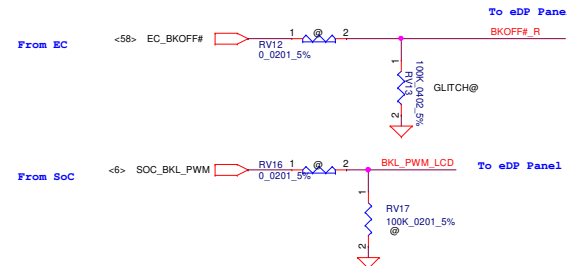
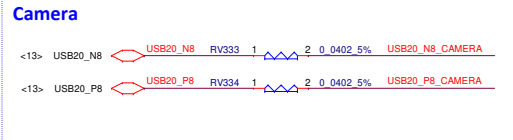
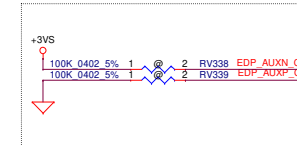
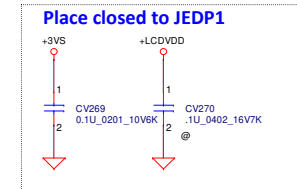
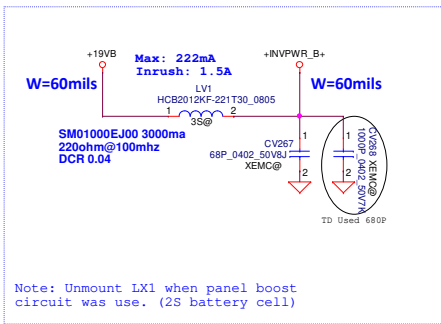
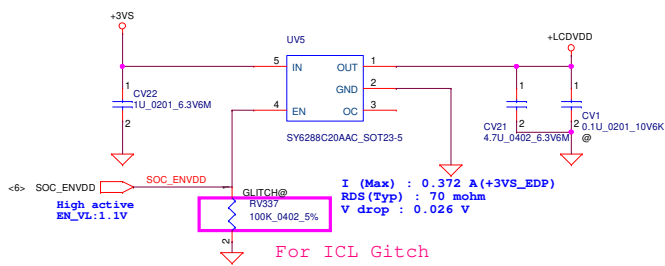
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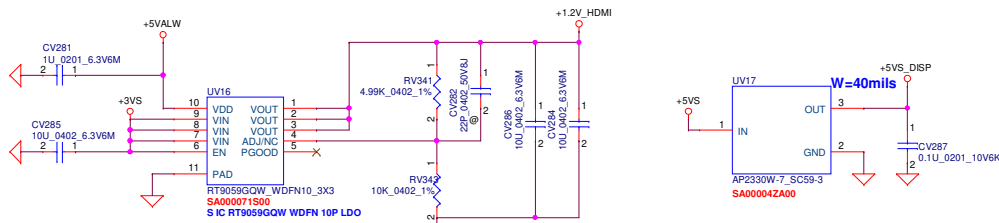
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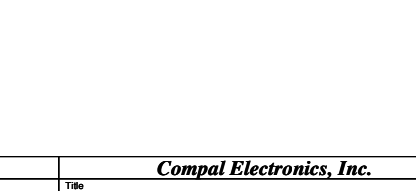
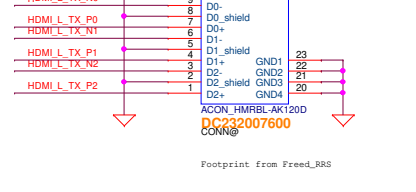
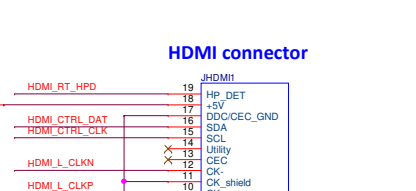
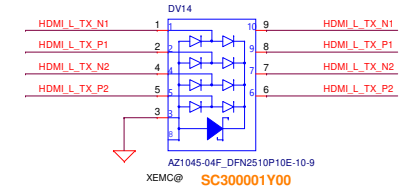
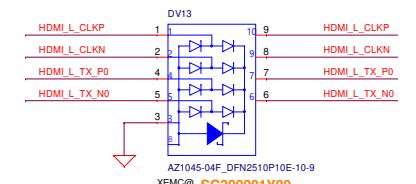
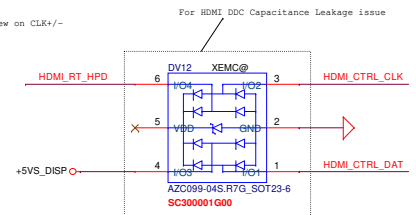
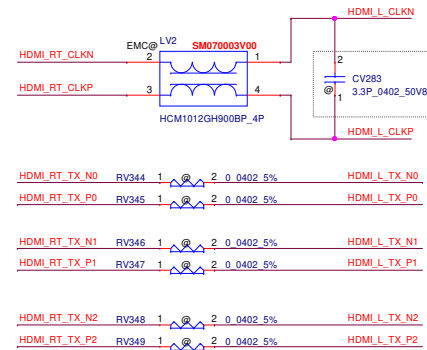
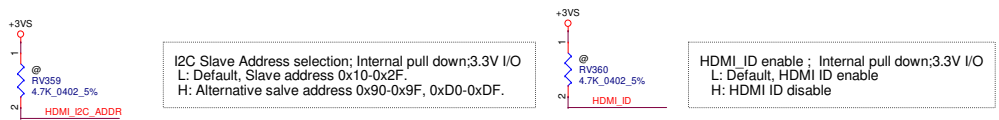
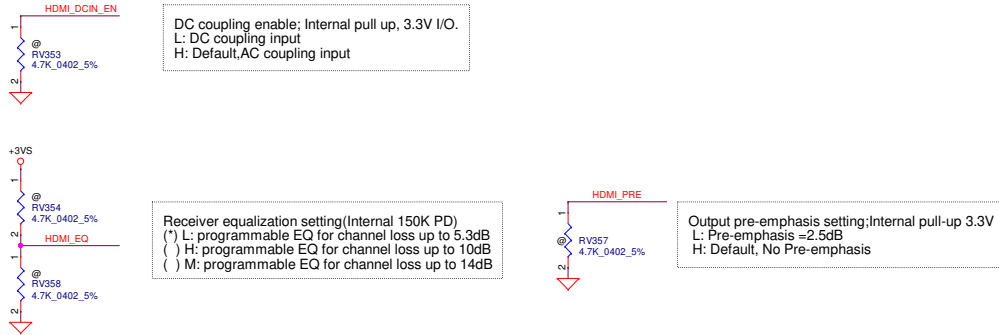
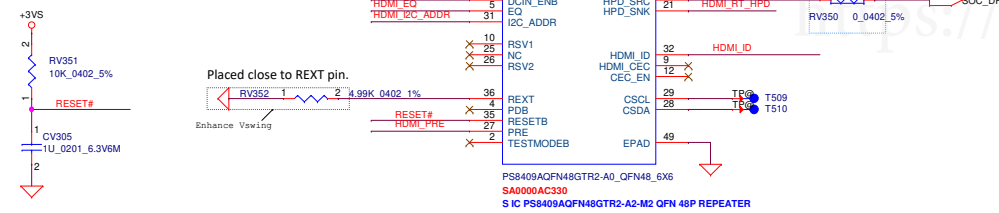
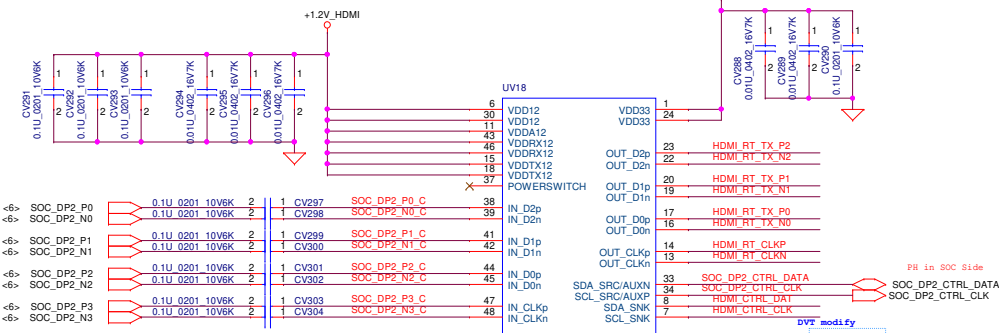


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Z772

HDMI ROYALTY
ROYALTY HDMI WLOGO+HDCP
RC0000003HM
45@



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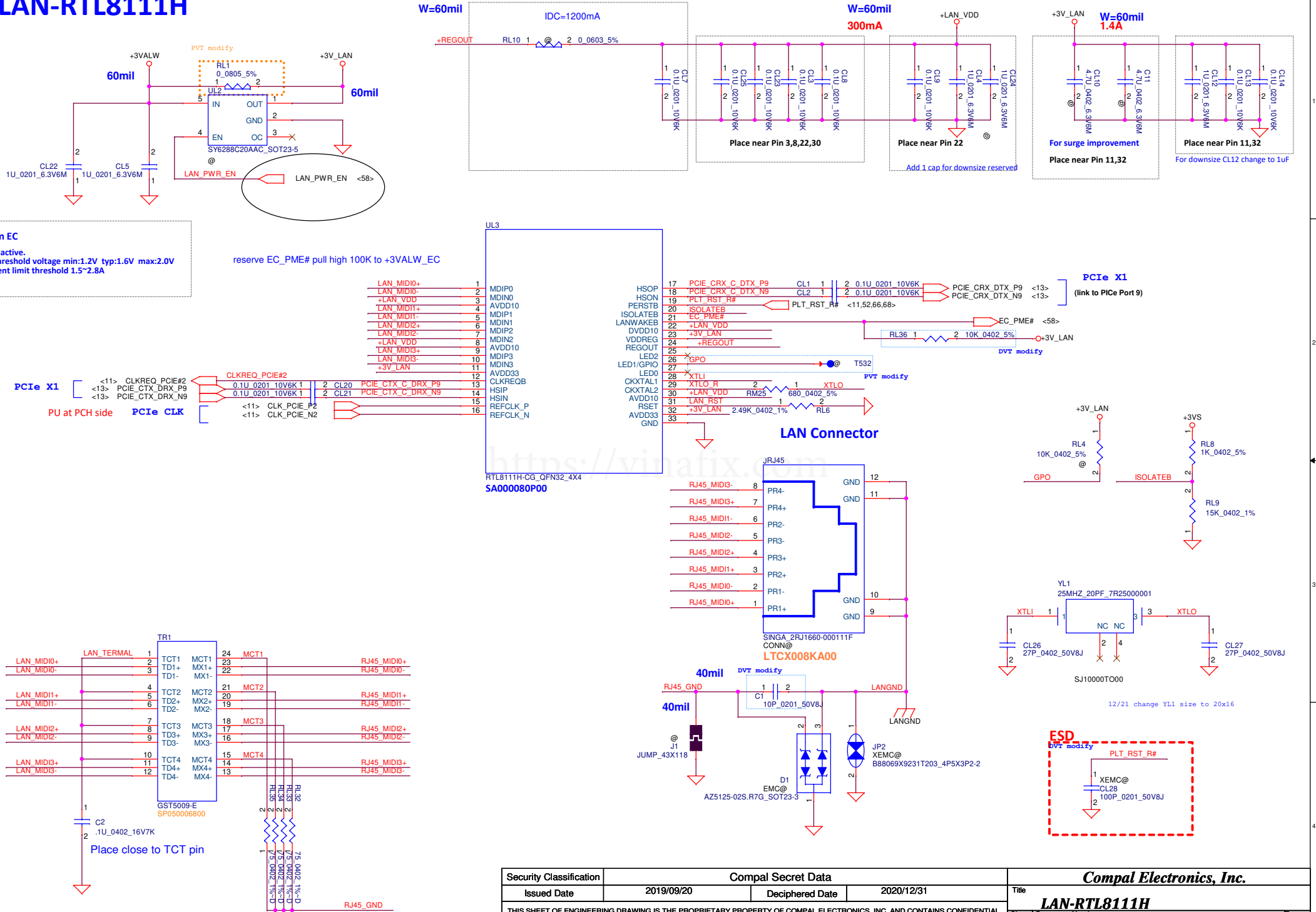
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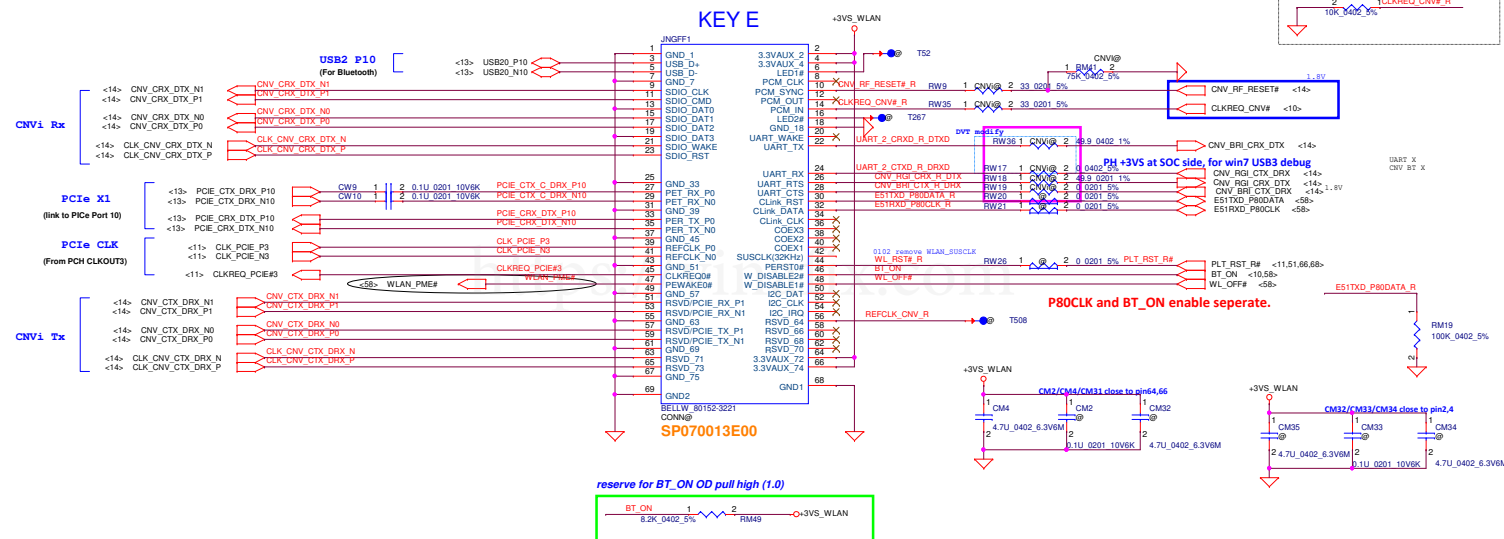
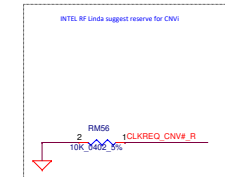
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LAN-RTL8111H



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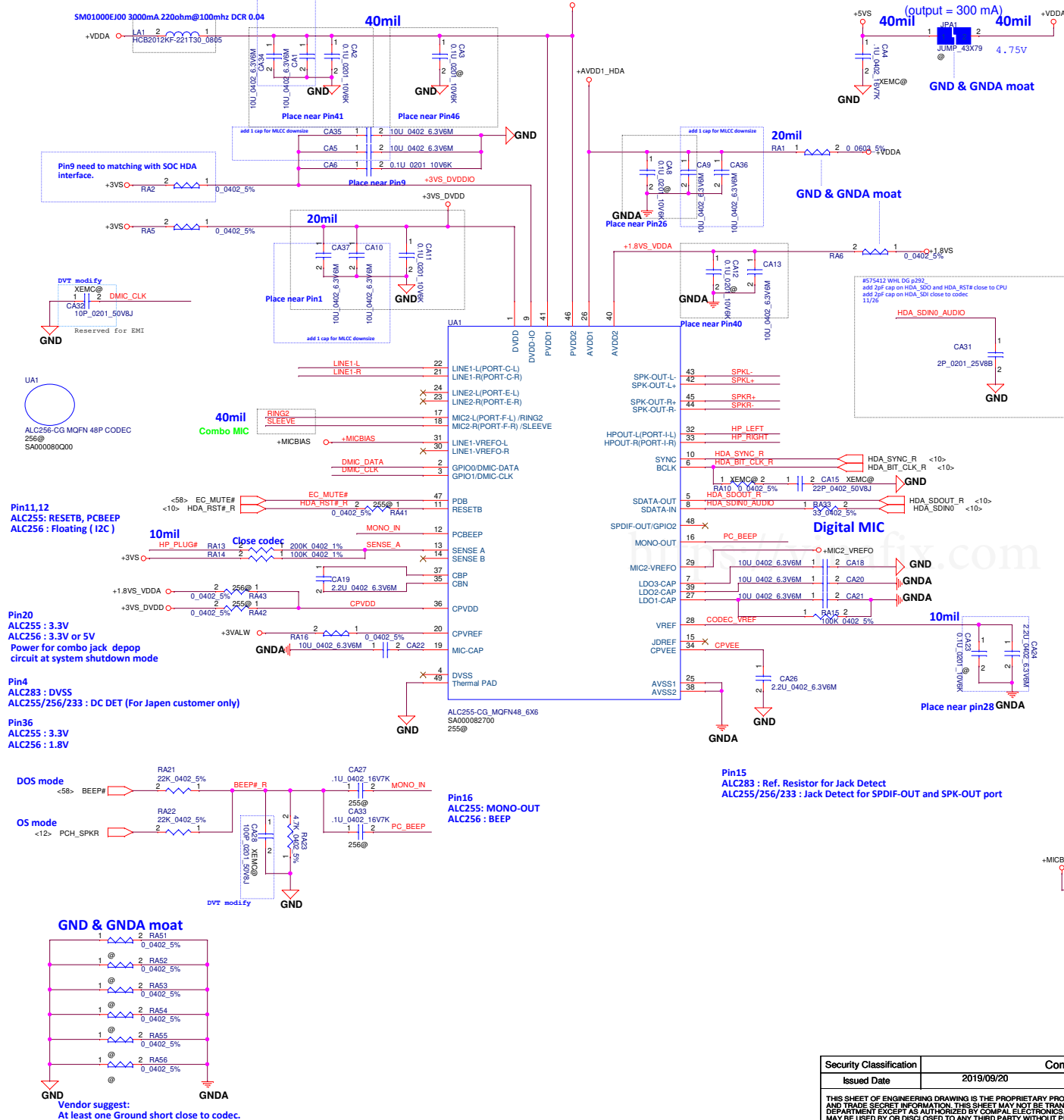
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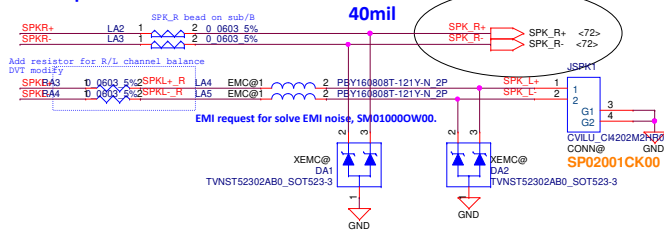
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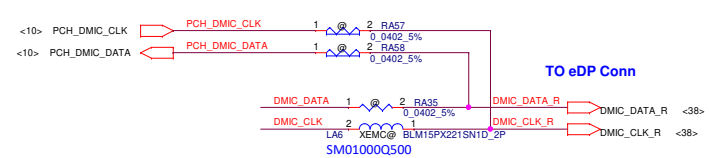
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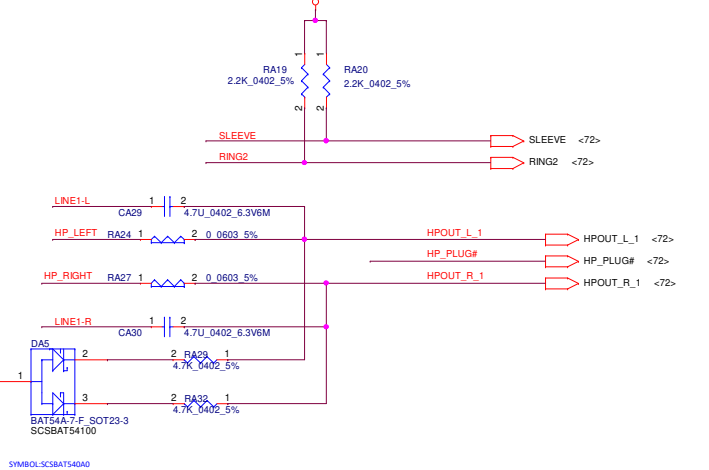
Int. Speaker Conn.



Digital MIC



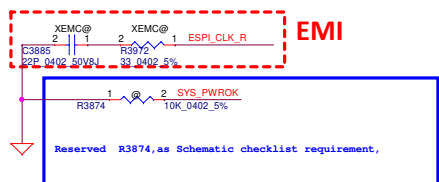
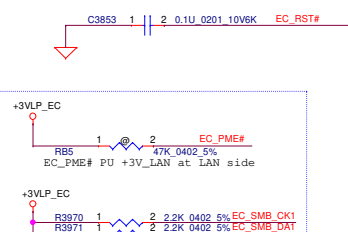
Headphone Out



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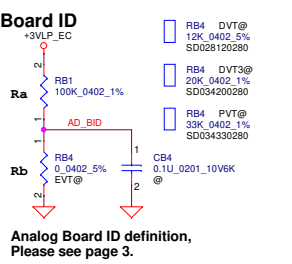
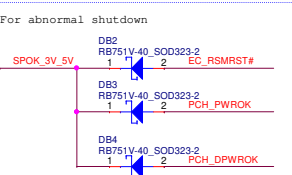
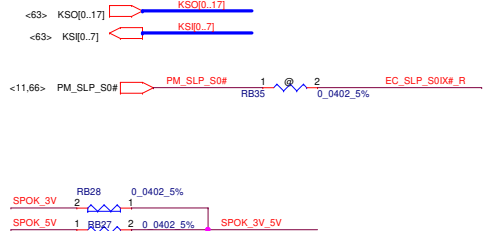
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OPMODE (Internal Pull High) :
Pull Up : Intel eSPI Master Attached Flash Sharing Topology
-> For KB9042 / KB9052

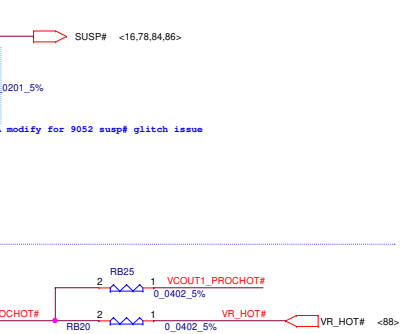
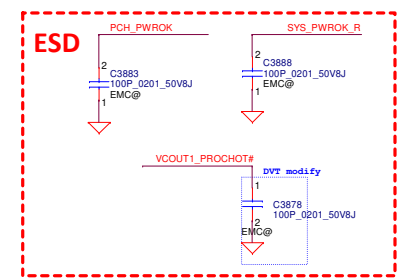
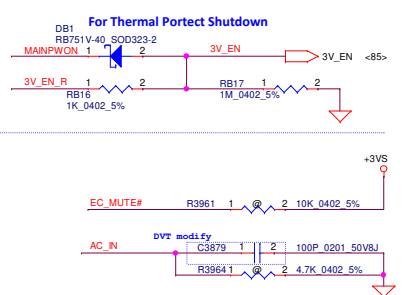
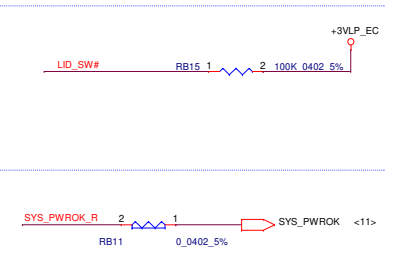
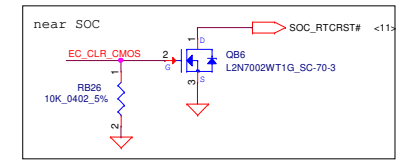
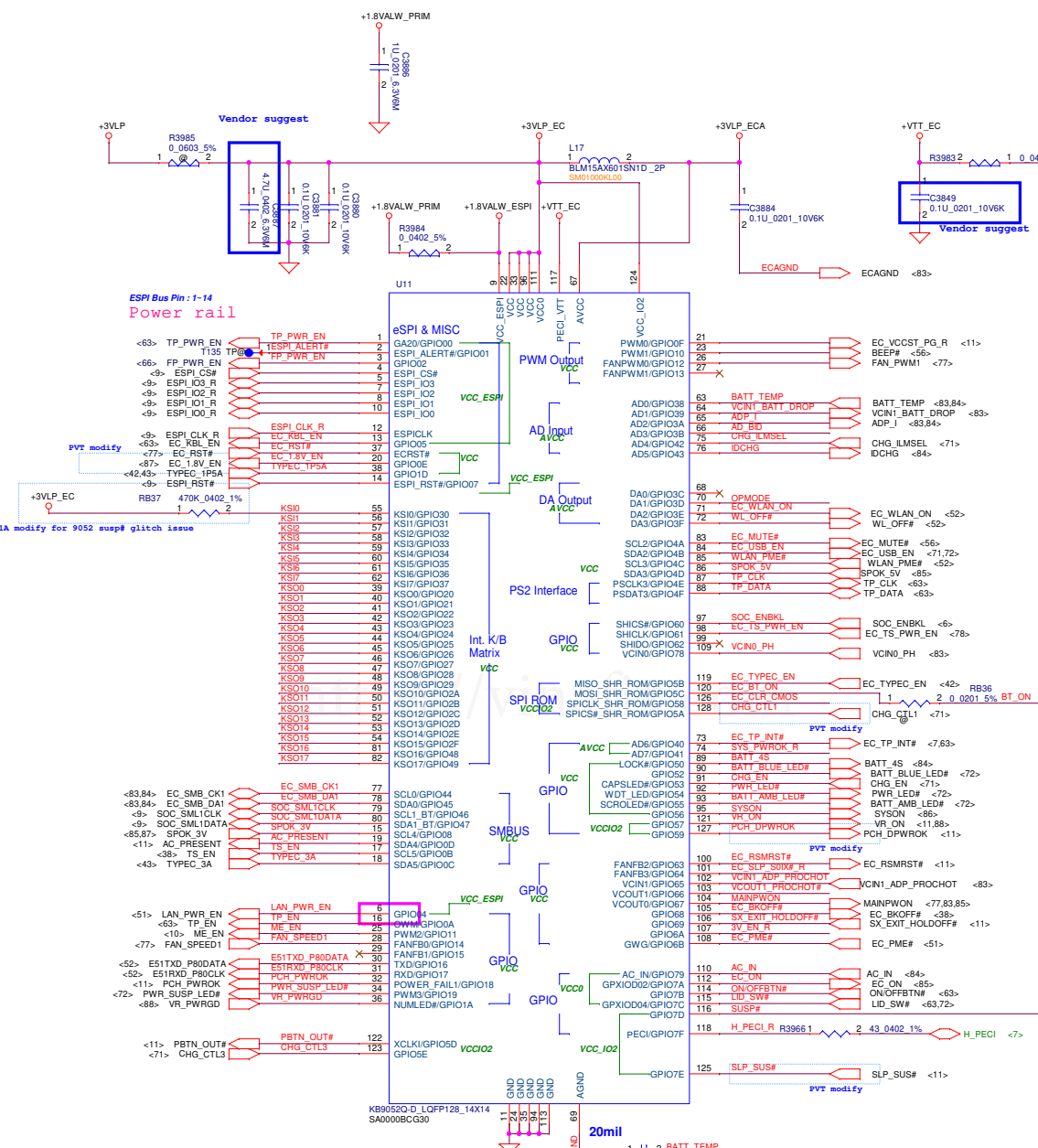
Pull Down : Intel Legacy Wire-OR share ROM.
-> For KB9022/9042 Use



IO pin groups v.s Power planes:

Power plane	Voltage	Pin#	Output Pin Power Rail	Input Pin VIH/VIL
VCC0	3.3V~2.0V(min) for PLC operation and data retention	110, 112, 114, 115	Push-pull @ VCC0 Open-Drain up to 5V	ref. to VCC0
VCC	3.3V only	15-62 77-109	Push-pull @ VCC Open-Drain up to 5V	ref. to VCC
VCC_ESPI	1.8V	1-14	Push-pull @ VCC_ESPI Open-Drain up to 5V	ref. to VCC_ESPI
AVCC	3.3V only	63-76 (102~109)*	Push-pull @ AVCC Open-Drain up to 5V	ref. to AVCC
VCC_I02	1.8V or 3.3V	116, 118-128	Push-pull @ VCC_I02 Open-Drain up to 5V	ref. to VCC_I02
PECL_Vtt	External applied Vtt	117		

Note *: pin-109(VGIN0) can be programmable internally connected to ADC ch8 (ADC8) and pin-102 (VCIN1) to ch9 (ADC9) by setting ADEN2[5:4]. If so, the voltage level on these two pins should not be higher than AVCC to prevent leakage.



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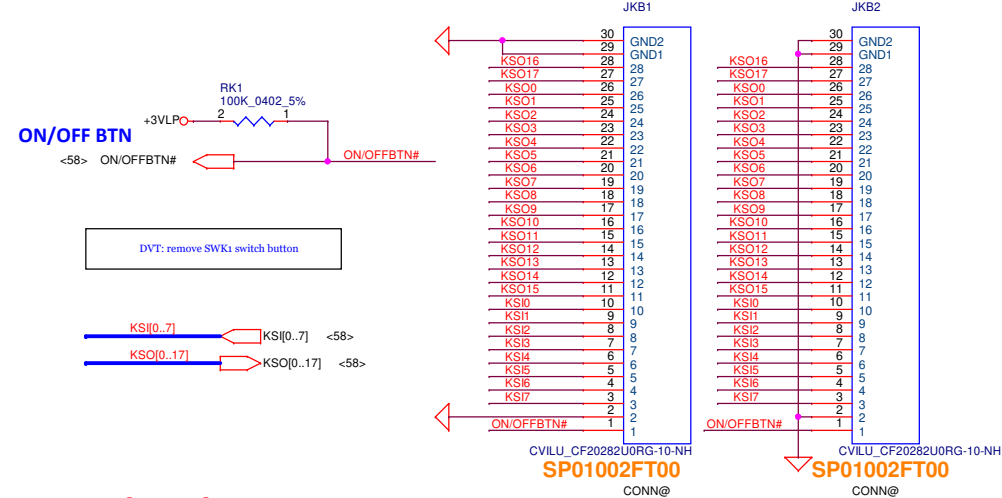
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					LA-K091P
				Date:	Wednesday, July 08, 2020
				Sheet	61 of 102
				Rev	0.1

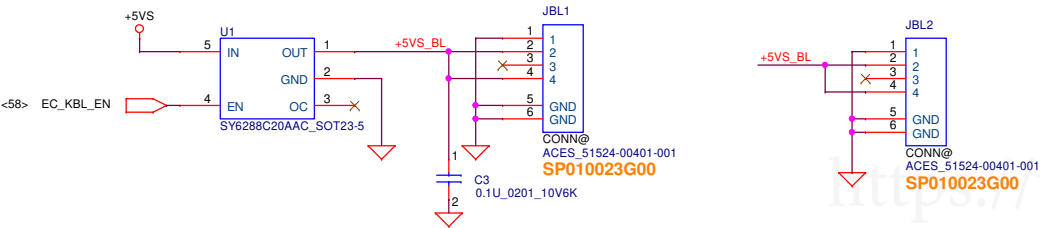
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					LA-K091P
				Date:	Wednesday, July 08, 2020
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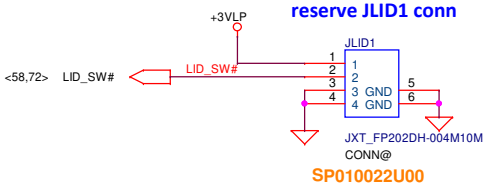
KB Conn.



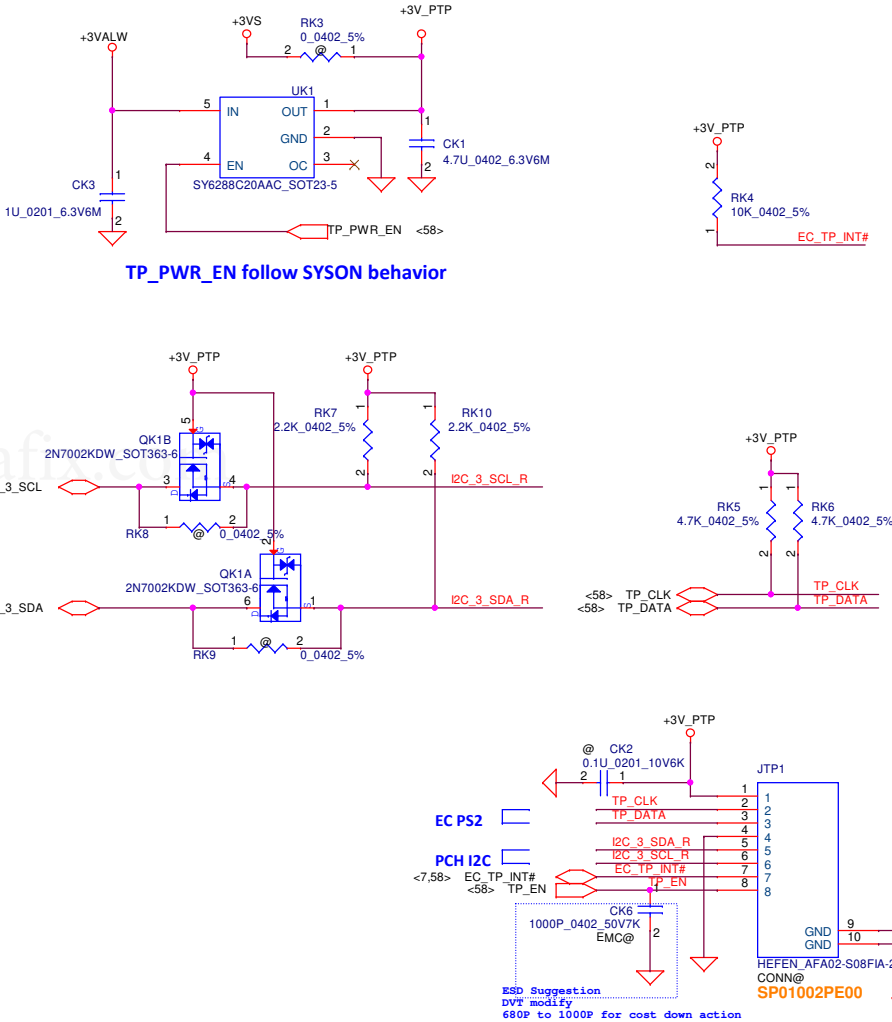
KB BackLight



Lid Switch



TP/B Conn.



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Issued Date	2017/11/23	Deciphered Date	2018/09/01	Title	KB/TP
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				Date: Wednesday, July 08, 2020	Sheet 63 of 102

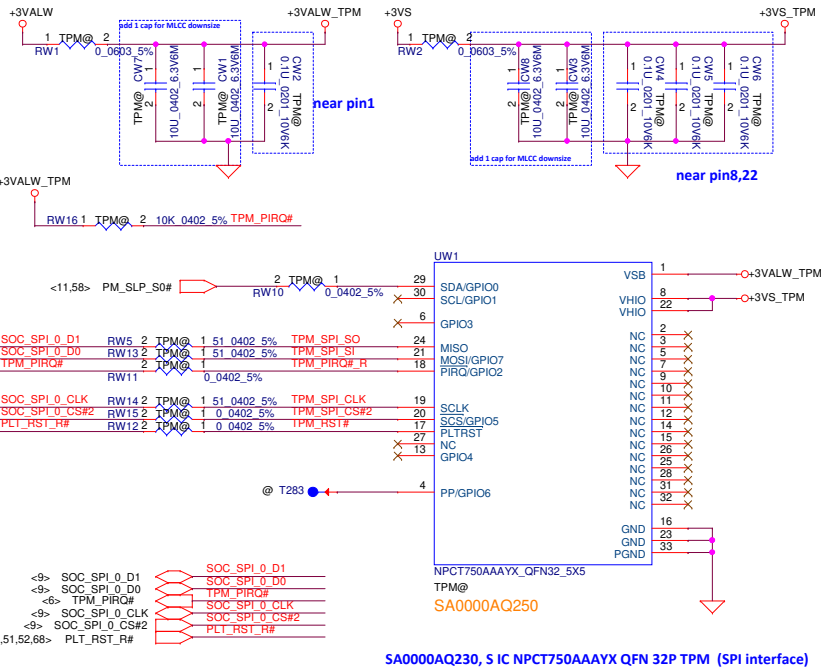
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	Reserve for KB/TP/LED/LID
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					LA-K091P
				Date:	Wednesday, July 08, 2020
				Sheet	64 of 102
				Rev	0.1

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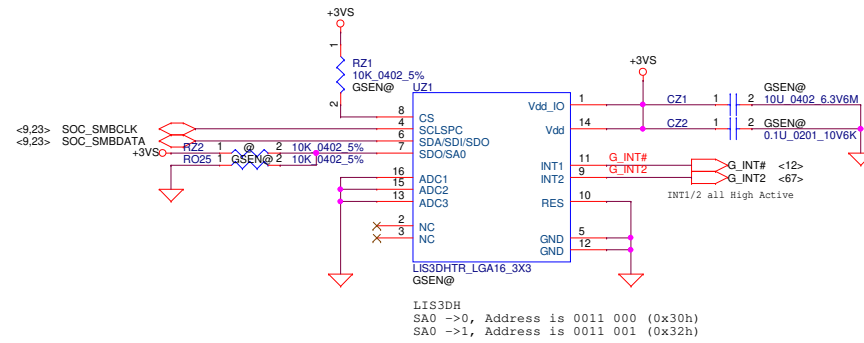
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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	Reserve for KB/TP/LED/LID
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					LA-K091P
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TPM 2.0



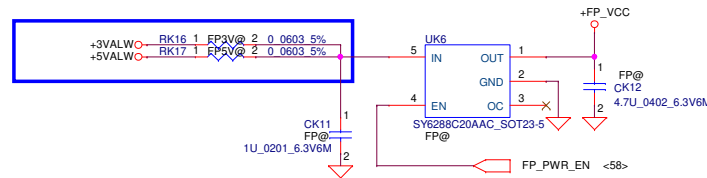
SA0000AQ230, S IC NCT750AAAYX_QFN 32P TPM (SPI interface)

G-Sensor reserved for BA serial

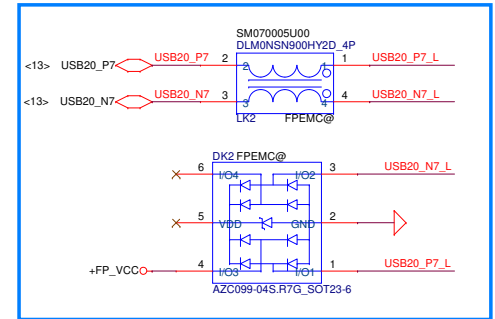
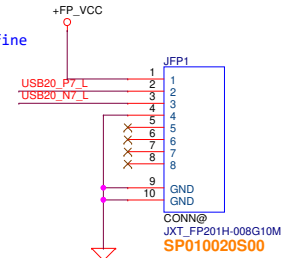


Finger Print

Power Source Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V

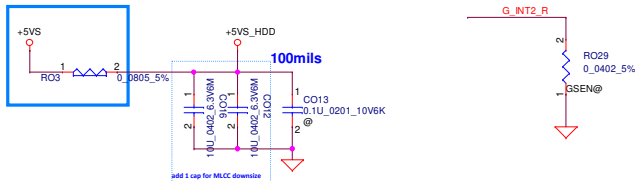


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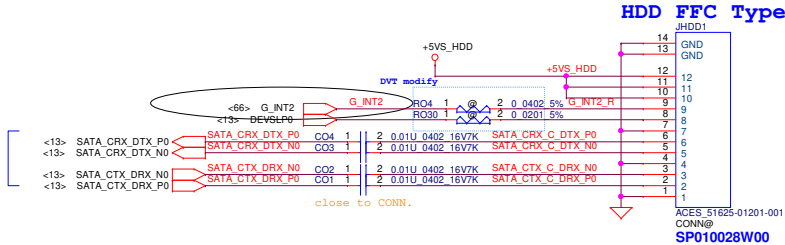


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				Document Number	Rev
				LA-K091P	1.0
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SATA HDD

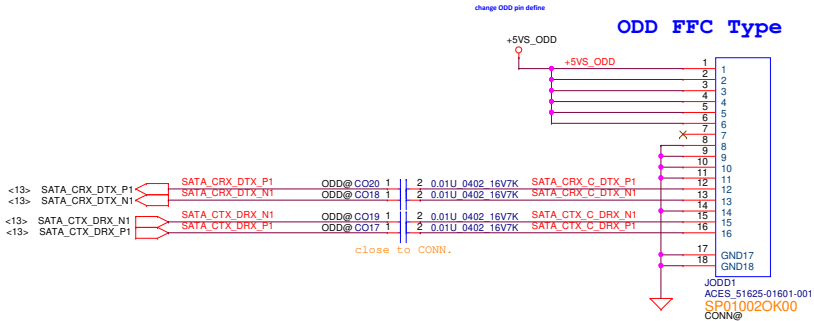
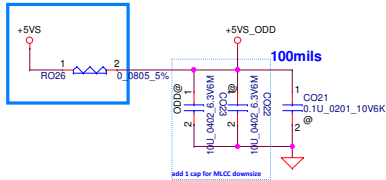


SATA Port 0

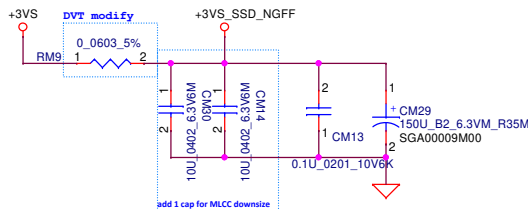


<https://vinafix.com>

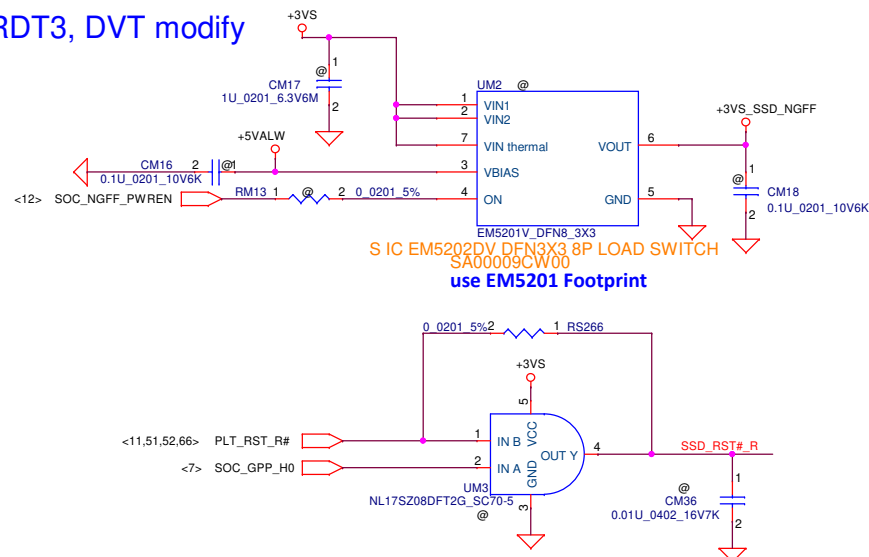
SATA ODD



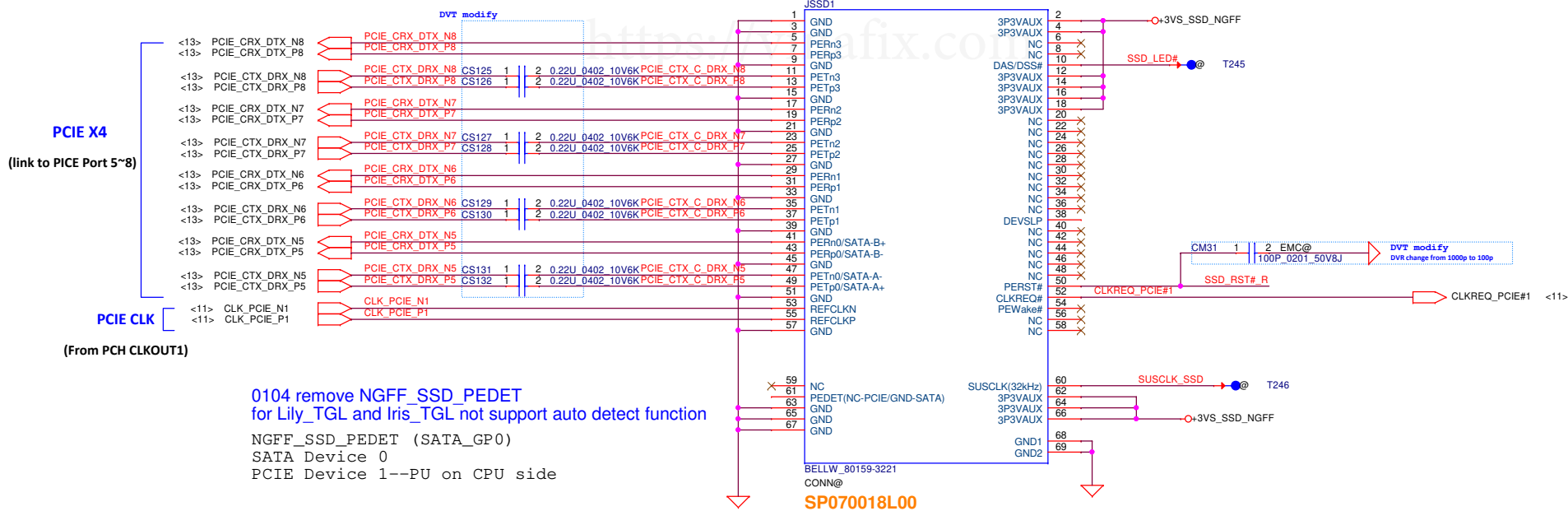
mSATA/SSD



reserve for RDT3, DVT modify



KEY M



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	NGFF SSD(KEY M)
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				Date	Wednesday, July 08, 2020
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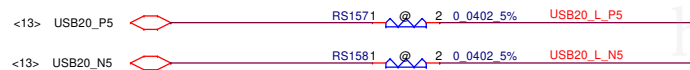
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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	Reserve eMMC
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<https://vinafix.com>

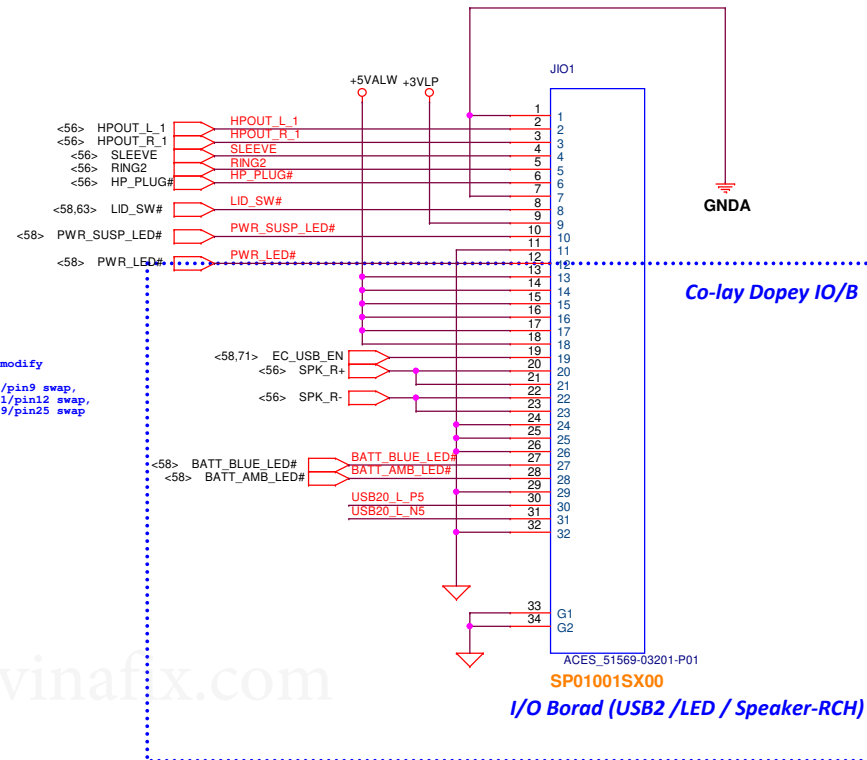
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USB2 I/O



Reserved CMC on SUB/B side

DVT modify
JIO1
pin8/pin9 swap,
pin11/pin12 swap,
pin19/pin25 swap



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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	Reserve USB2/USB3 TYPEA
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Issued Date	2019/09/20	Deciphered Date	2020/12/31	Title	Reserve USB2/USB3 DB
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					LA-K091P
				Date:	Wednesday, July 08, 2020
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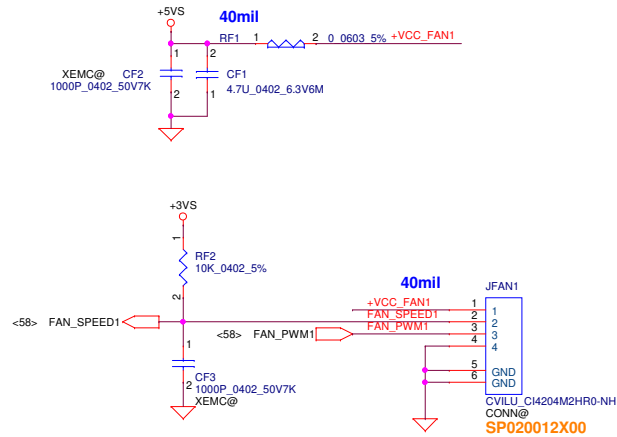
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				Date:	Wednesday, July 08, 2020
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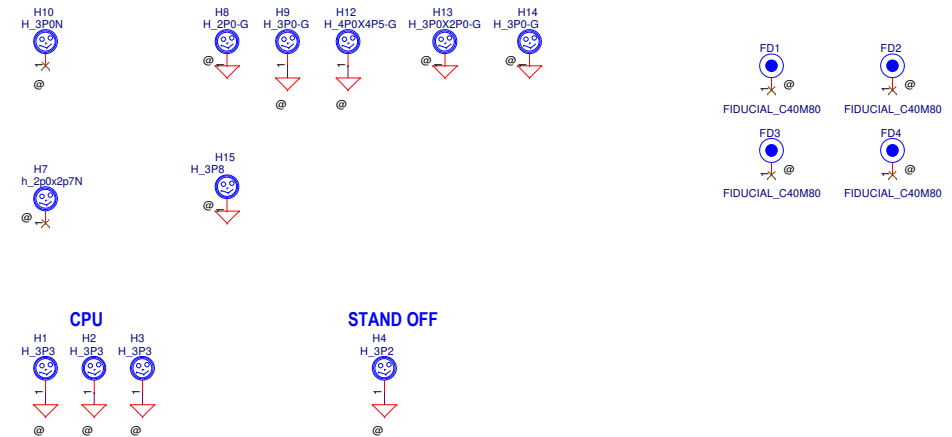
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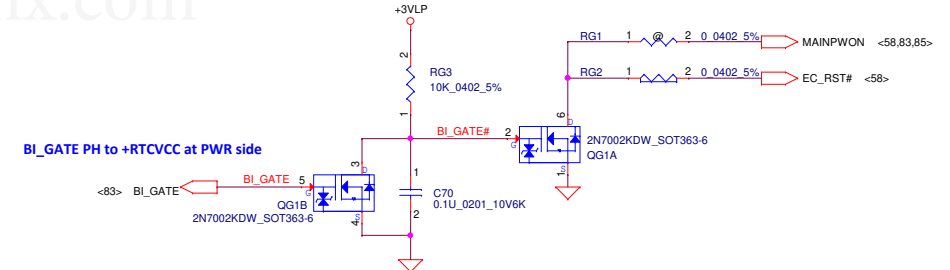
FAN1 Conn



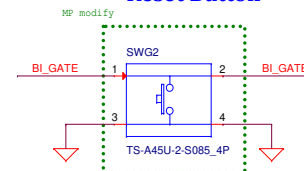
Screw Hole



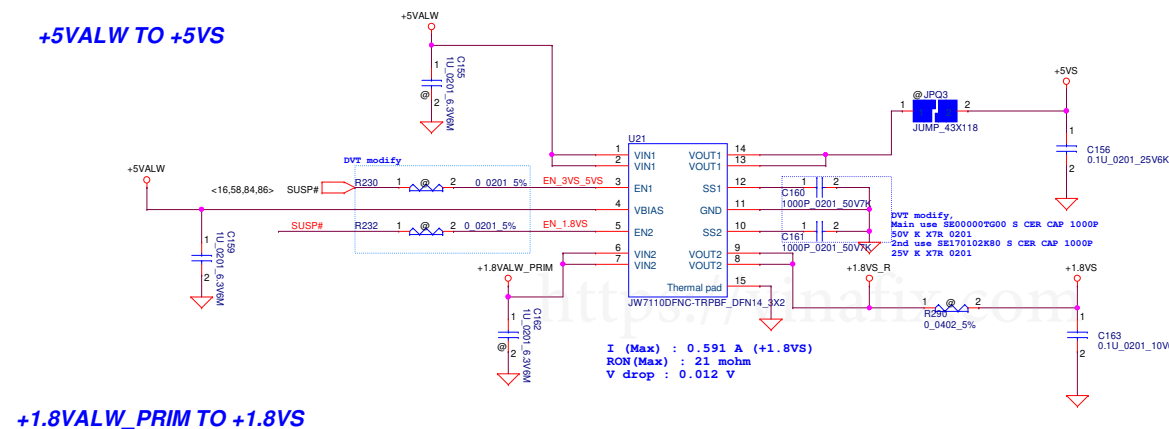
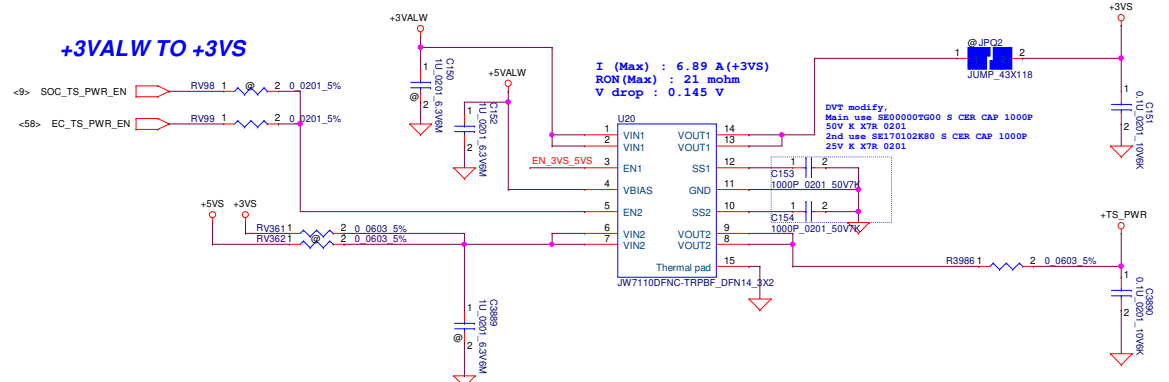
Reset Circuit



Reset Button



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+1.8VALW_PRIM TO +1.8VS

DIS (1.8VSDGPU_AON and +1.8VSDGPU_MAIN), remove

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				Date:	Wednesday, July 08, 2020
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				Rev	0.1

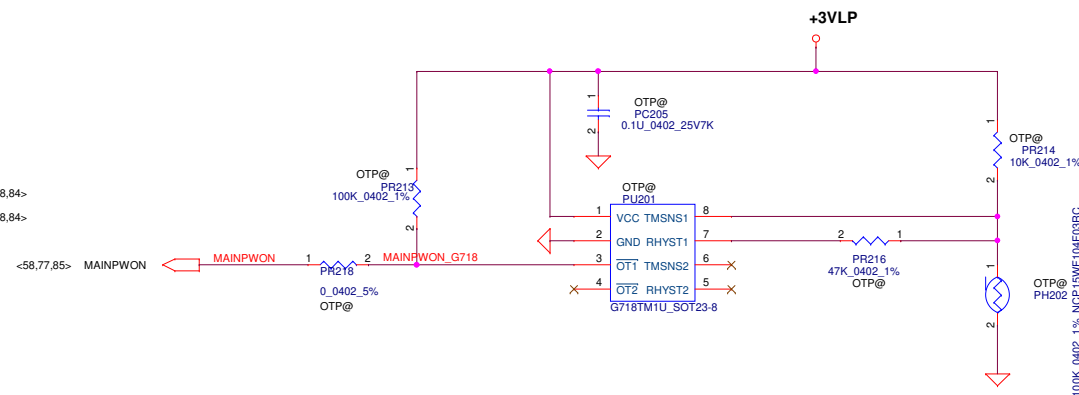
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Security Classification	Compal Secret Data			Title	
Issued Date	2019/09/20	Deciphered Date	2020/12/31	FIP Conn	
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PWR-Reserve Page

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Title <Title>			
Size A	Document Number LA-K091P		Rev 0.1
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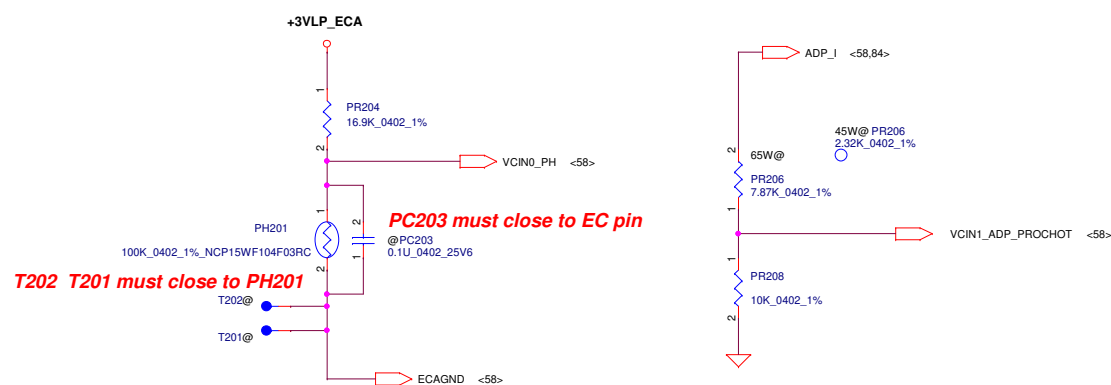


For KB9022 sense 20m	Active	Recovery
45W PR206 2.32K ohm	58.5W, 1V	Active=recovery
65W PR206 7.87K ohm	84.5W, 1V	Active=recovery
90W PR20K ohm	___W, ___V	Active=recovery
PH1	2V	1V

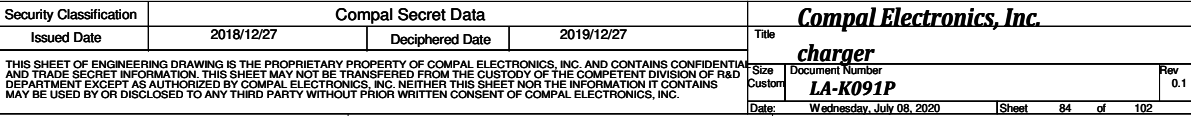
design.

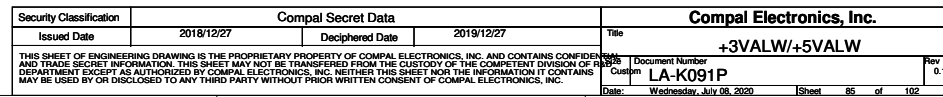
NVDC design

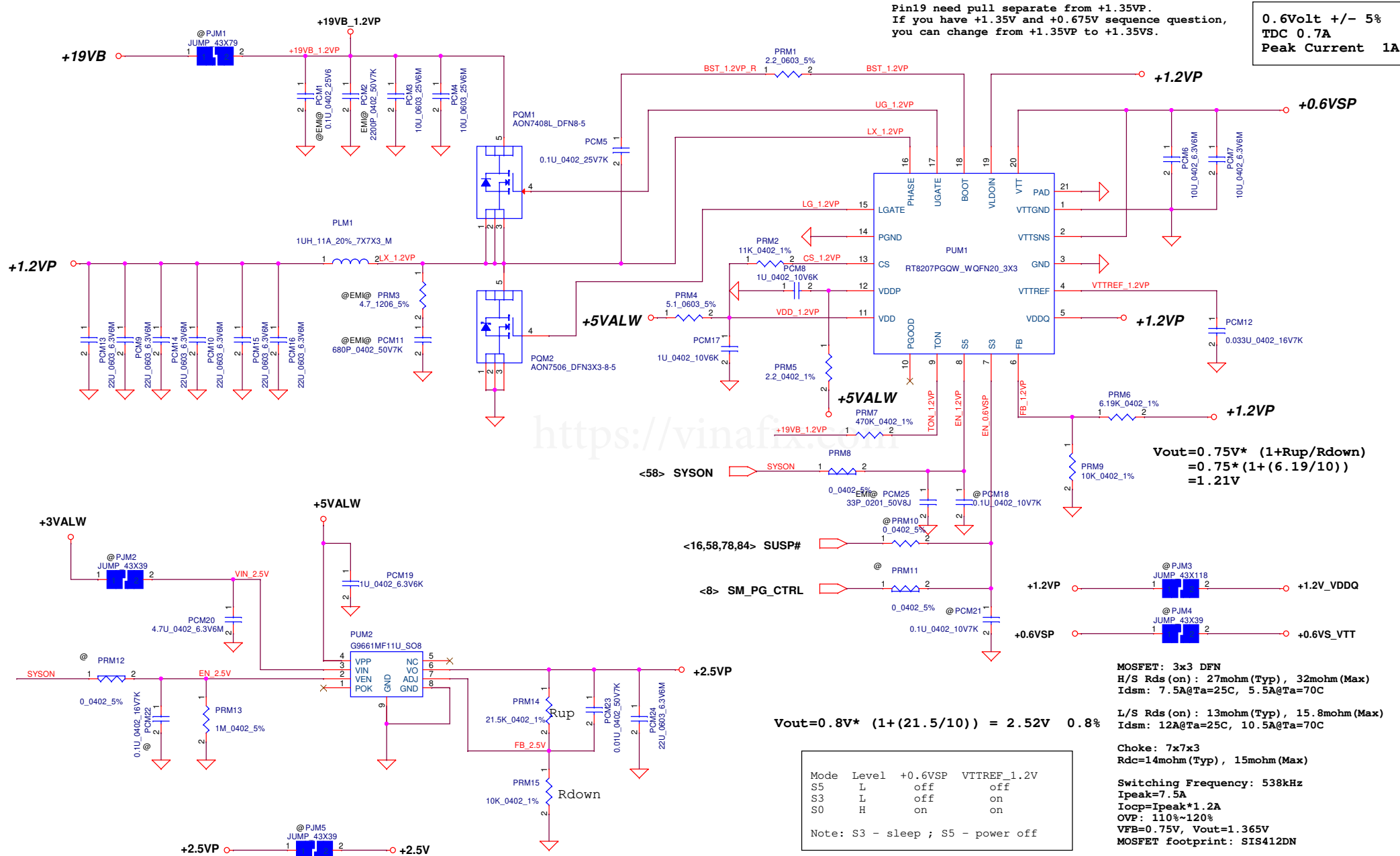
The diagram shows a circuit for NVDC design. It features a voltage divider network connected to a +19VB_5V supply. The divider consists of two resistors, PR209 (750K_0402_1%) and PR211 (150K_0402_1%), connected in series. A load resistor, PR210 (0_0402_5%), is connected in parallel with PR211. The output of the divider is labeled VCIN1_BATT_DROP <58>. A capacitor, PC204 (0.1U_0402_25V6), is connected in parallel with the divider network. The circuit is powered by a +19VB_5V supply.



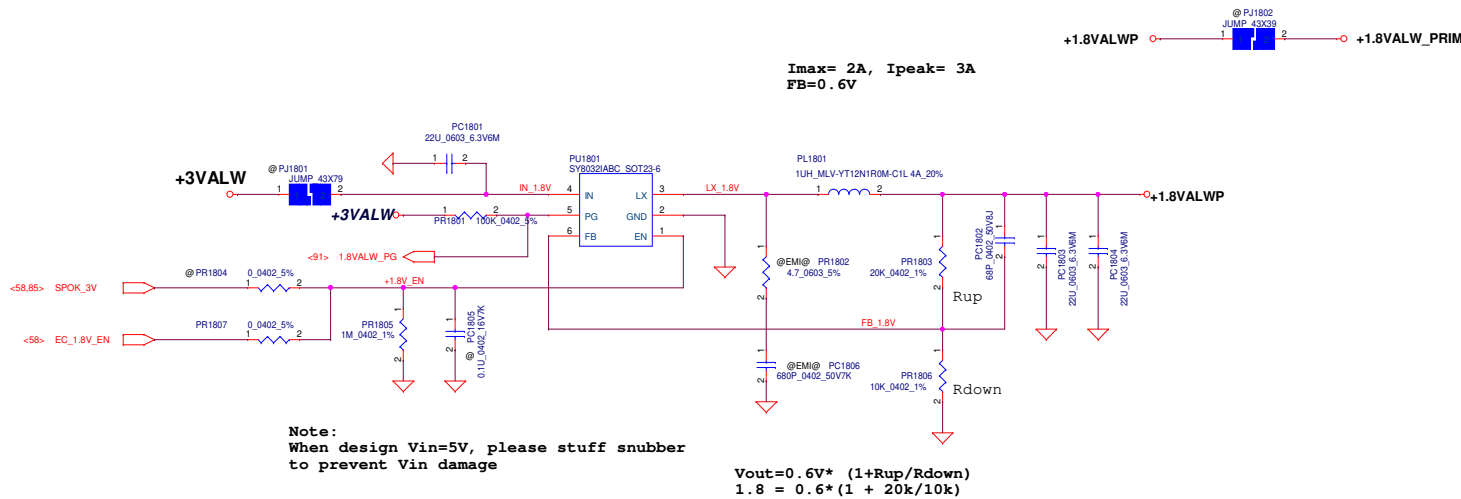
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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title		
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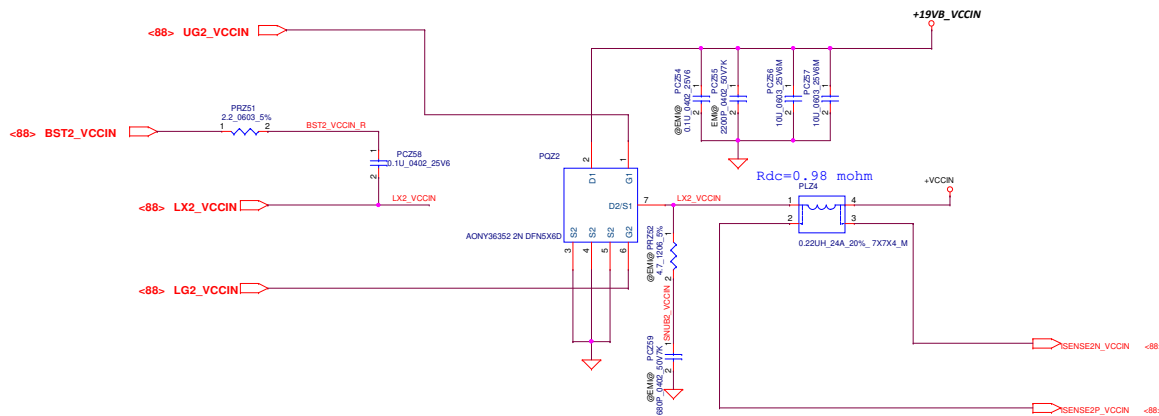
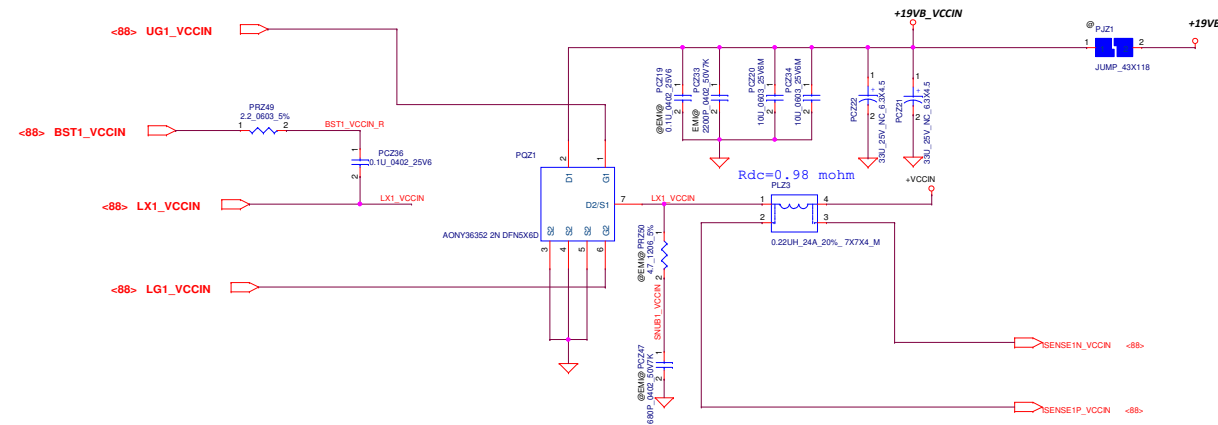
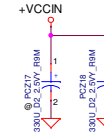
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Issued Date	2018/12/27	Deciphered Date	2019/12/27	Title	SY8032
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RT3612EB_2Phase_V1B.mdd for SW portion

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Issued Date	2019/05/15	Deciphered Date	2020/05/15	Title	
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ICCMAX=54A
TDC=25A
OCP=160% of Iccmax=86.4A
OVP=VID+0.35V=2.24V

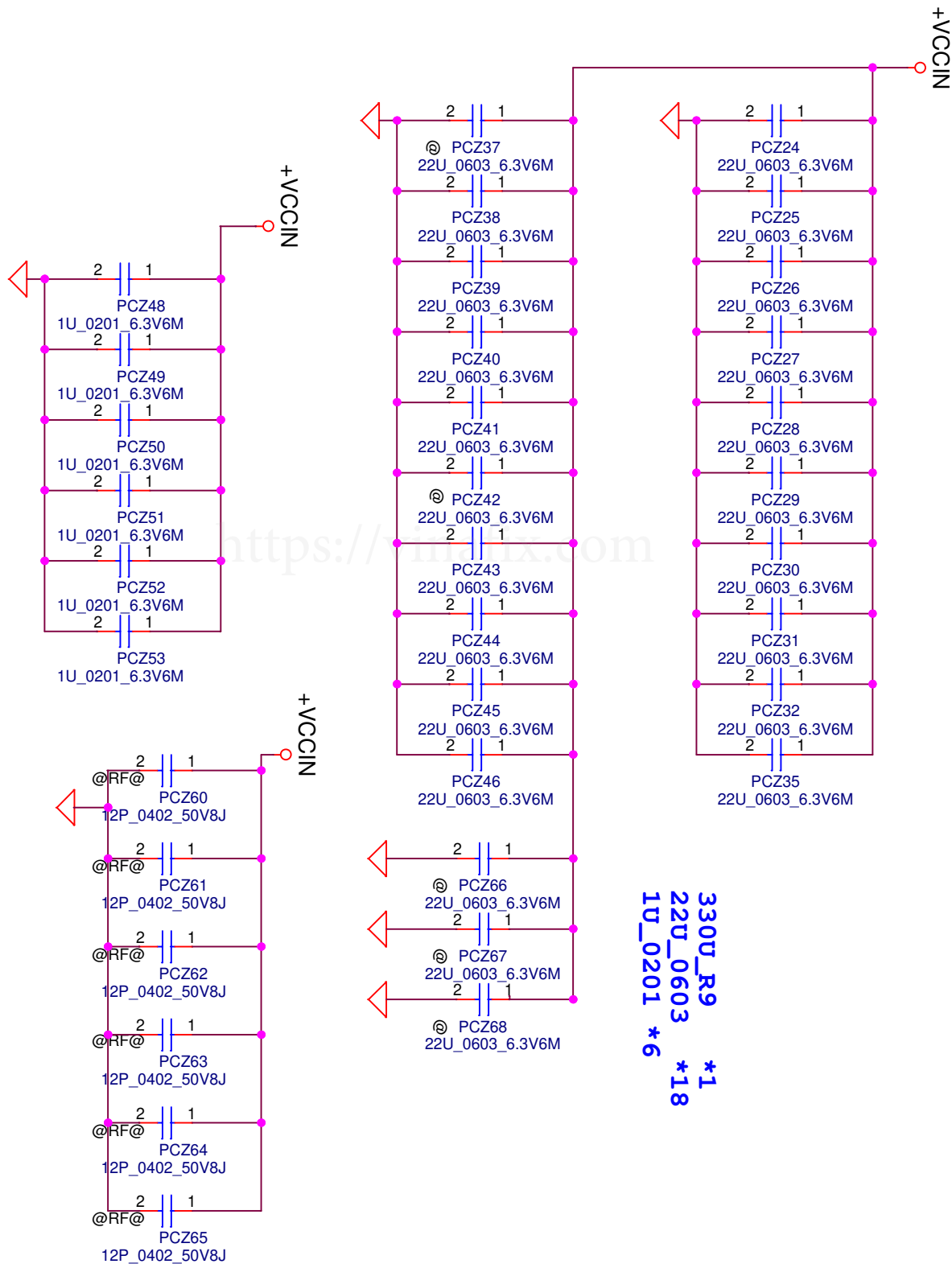
Frequency 600KHz



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Compal Electronics, Inc.
Power stage-VCCIN



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Module model information
RT6543A_V1A.mdd for IC portion
RT6543A_V1B.mdd for SW portion

OCp is Lowside MOSFET Rdson sense

226K x1.2
255K x1.4

+5VALW

High > 1V
Low < 0.4V

+3VALW

+5VALW

5V: 800KHz
Float: 600KHz
GND: 400KHz

VCCIN_AUX VID Follow Intel PDG Rev0.71

VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

+19VB

AUX input cap need place 5pcs

+19VB_AUX

+19VB

ICCMAX=31A
TDC=14A
DC LL=TBD
AC LL=4.5

Rdc=0.98 mohm

+VCCIN_AUX

+VCCIN_AUX

330U_R9 *1
22U_0603 *13

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01		New version charger		p84	Change PUB1 from BQ24781(SA0000A6B00) to BQ24800(SA000D7R00)	02/10	Pre-EVT
02		sourcer request		p91 p84 p82 p86 p83	Change PCG12 from 820P 25V K X7R 0402(SE000008980) to 820PF 50V K X7R 0402(SE000003W00) Change PCB18 from 2.2U 25V K X5R 0603(SE00000WP00) to 2.2U 16V K X5R 0603(SE000006S80) Change PC102 from 100P 50V J NPO 0402(SE071101J80) to 100P 50V J NPO 0201(SE00000SE00) Change PCM25 from 33P 50V J NPO 0402(SE071330J80) to 33P 50V J NPO 0201(SE00000TB00) Change PCM23,PCB13,PC202 from .01U 25V K X7R 0402(SE075103K80) to .01U 50V K X7R 0402(SE074103K80)	04/10	EVT
03		CPU transient test		p88	Change PRZ14 from 1.74K +-1% 0402(SD034174180) to 442_0402_1%(SD034442080) Change PRZ28 from 15K +-1% 0402(SD034150280) to 75K +-1% 0402(SD034750280) Change PRZ46 from 30.9K +-1% 0402(SD034309280) to 27K +-1% 0402(SD034270280)	04/10	EVT
04		CPU transient test		p88	Change PRZ9 from 750_0402_1% 0402(SD034750080) to 105K_0402_1%(SD034105380) Change PRZ26 from 680 +-1% 0402 (SD034680080) to 17.8K +-1% 0402(SD034178280) Change PCZ12 from 330P 50V K X7R 0402(SE074331K80) to 220P 50V K X7R 0402(SE074221K80)	06/09	DVT
05		0 ohm shortpad		p86 88 89	PRG9,PRM8,PRZ4 depop	06/09	DVT
06		1.8v Enable control , HW comfirm use PR1807 Del PR1804		p87	Pop PR1807, Depop PR1804	06/16	PVT
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